DATA TRANSLATION

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DT3010 Series User's Manual

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Data Translation, Inc.
100 Locke Drive
Marlboro, MA 01752-1192
(508) 481-3700
www.datatranslation.com
Fax: (508) 481-8620
E-mail: info@datx.com

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About this Manual

This manual describes the features of the DT3010, DT3010-268, DT3010/32, DT3010/32-268, and DT3016 boards (collectively referred to as the DT3010 Series), the capabilities of the DT3010 Series Device Driver, and how to program the DT3010 Series board using DT-Open Layers™ software. Troubleshooting and calibration information is also provided.

Intended Audience

This document is intended for engineers, scientists, technicians, or others responsible for using and/or programming the DT3010 Series boards for data acquisition operations in Microsoft® Windows® 98, Windows Me (Millennium Edition), Windows NT® 4.0, Windows 2000, or Windows XP. It is assumed that you have some familiarity with data acquisition principles, and that you understand your application.

What You Should Learn from this Manual

This manual provides detailed information about the features of the DT3010 Series boards and the capabilities of the DT3010 Series Device Driver. It is organized as follows:

- Chapter 1, "Overview," describes the major features of the board, as well as the supported software and accessories for the board.
- Chapter 2, "Principles of Operation," describes all of the board's features and how to use them in your application.
- Chapter 3, "Supported Capabilities," lists the data acquisition subsystems and the associated features accessible using the DT3010 Series Device Driver.

- Chapter 4, "Programming Flowcharts," describes the processes you must follow to program the subsystems on the DT3010 Series board using DT-Open Layers-compliant software.
- Chapter 5, "Calibration," describes how to calibrate the analog I/O circuitry of the board.
- Chapter 6, "Troubleshooting," provides information that you can use to resolve problems with the board and the device driver, should they occur.
- Appendix A, "Specifications," lists the specifications of the board.
- Appendix B, "Connector Pin Assignments," shows the pin assignments for the connectors on the board and for the DT740, STP268, and STP268-EC screw terminal panels.
- An index completes this manual.

Conventions Used in this Manual

The following conventions are used in this manual:

- Notes provide useful information or information that requires special emphasis, cautions provide information to help you avoid losing data or damaging your equipment, and warnings provide information to help you avoid catastrophic damage to yourself or your equipment.
- Items that you select or type are shown in **bold**.

Related Information

Refer to the following documents for more information on using the DT3010 Series board:

- *DT3010 Series Getting Started Manual* (UM-16868). This manual describes how to install the DT3010 Series boards, support software, and device driver; verify the operation of the board; and view the DT3010 Series documentation online. This manual is provided on the Data Acquisition OMNI CD™.
- *DT Measure Foundry Getting Started Manual* (UM-19298) and online help. These documents describe how to use DT Measure Foundry™ to build drag-and-drop test and measurement applications for Data Translation® data acquisition devices without programming.
- *DataAcq SDK User's Manual* (UM-18326). For programmers who are developing their own application programs using the Microsoft C compiler, this manual describes how to use the DT-Open Layers DataAcq SDK™ to access the capabilities of Data Translation data acquisition boards. This manual is provided on the Data Acquisition OMNI CD.
- *DTx-EZ Getting Started Manual* (UM-15428). This manual, available from Data Translation, describes how to use the ActiveX controls provided in DTx-EZ™ to access the capabilities of Data Translation data acquisition boards in Microsoft® Visual Basic™ or Visual C++.
- *DT VPI User Manual* (UM-16150). This manual, available from Data Translation, describes how to use DT VPI™ and the Agilent® VEE™ visual programming language to access the capabilities of Data Translation data acquisition boards.
- *DT-LV Link Getting Started Manual* (UM-15790). This manual, available from Data Translation, describes how to use DT-LV Link™ with the LabVIEW® graphical programming language to access the capabilities of Data Translation data acquisition boards.

- *PCI Specification:* PCI Local Bus Specification, PCI Special Interest Group, Portland, OR. (Revision 2.1, June 1, 1995).
- Microsoft Windows 98, Windows Me, Windows NT 4.0, Windows 2000, or Windows XP user manuals.

Where To Get Help

Should you run into problems installing or using a DT3010 Series board, our Technical Support Department is available to provide prompt, technical assistance. Refer to Chapter 6 for more information. If you are outside the U.S. or Canada, call your local distributor, whose number is listed in your Data Translation product handbook.

1

Overview

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Features

The DT3010 Series consists of the following high-speed, multifunction board types for the PCI bus: DT3010, DT3010-268, DT3010/32, DT3010/32-268 and DT3016. These board types differ in analog I/O resolution, output FIFO (first-in, first-out buffer) size, throughput, D/A filters, and connectors as shown in Table 1.

Table 1: Differences Among DT3010 Series Boards

Board Type	Analog I/O Resolution	Output FIFO Size	A/D Throughput[a]	D/A Throughput[b]	D/A Filters	Connectors
DT3010	12 bits	4 kSamples	1.25 MSamples/s	200 kSamples/s	–	one 50-pin, one 68-pin
DT3010 -268	12 bits	4 kSamples	1.25 MSamples/s	200 kSamples/s	–	two 68-pin
DT3010 /32	12 bits	32 kSamples	1.25 MSamples/s	200 kSamples/s	–	one 50-pin, one 68-pin
DT3010 /32-268	12 bits	32 kSamples	1.25 MSamples/s	200 kSamples/s	–	two 68-pin
DT3016	16 bits	4 kSamples	250 kSamples/s	100 kSamples/s	0 and 20 kHz	one 50-pin, one 68-pin

a. This throughput is for a single analog input channel.
b. This throughput is for full-scale ranges.

All DT3010 Series boards share the following major features:

- 32 Single-ended or pseudo-differential analog input channels, or 16 differential analog input channels;
- Programmable bipolar (±10 V) and unipolar (0 to 10 V) input ranges with gains of 1, 2, 4, and 8;

- Continuously-paced and triggered scan capability;
- A 1024-location channel-gain list that supports sampling analog input channels at the same or different gains in sequential or random order;
- Up to 256 scans per trigger for a total of 262,144 samples per trigger;
- PCI bus mastering for data transfers;
- Pre-, post-, and about-trigger acquisition modes to acquire data relative to an external event using computer memory;
- Internal and external clock sources; one external clock input for the analog input subsystem and one external clock input for the analog output subsystem;
- Analog threshold triggering using either an external analog input or one of the analog input channels; a separate DAC sets the trigger level (8-bit resolution, fixed hysteresis);
- Digital TTL triggering; one external hardware TTL input for the analog input subsystem and one external hardware TTL input for the analog output subsystem;
- Two analog output channels with a ±10 V output range;
- Simultaneous analog input and analog output operations running at full speed;
- Software calibration of the analog input and output subsystems;
- Two 8-bit digital ports programmable as inputs or outputs on a per-port basis; digital inputs can be included as part of the analog input channel-gain list to correlate the timing of analog and digital events; digital outputs can drive external solid-state relays;
- Two dynamic, high-speed digital output lines; useful for synchronizing and controlling external equipment, these dynamic digital output lines are programmable as part of the analog input subsystem;

- Four user counter/timers programmable for event counting, frequency measurement, rate generation (continuous pulse output), one-shot pulse output, and repetitive one-shot pulse output;
- Programmable gate types;
- Programmable pulse output polarities (output types) and duty cycles; and
- A/D Sample Clock Output and A/D Trigger Output signals, useful for synchronizing and controlling external equipment.
- For a discussion of these features in detail, refer to Chapter 2.

Supported Software

The following software is available for use with the DT3010 Series boards:

- **DT3010 Series Device Driver** – This software is included on the Data Acquisition OMNI CD that is shipped with the board. You *must* install this DT3010 Series software, which installs the device driver, to use the DT3010 Series board with any of the supported software packages or utilities. Refer to the *DT3010 Series Getting Started Manual* (UM-16868) for more information on installing the software.
- **The Quick Data Acq application** – This software is shipped with the board on the Data Acquisition OMNI CD. This application provides a quick way to get a DT3010 Series board up and running. Using the Quick Data Acq application, you can verify the features of the board, display data on the screen, and save data to disk. Refer to the *DT3010 Series Getting Started Manual* (UM-16868) for information on using the Quick Data Acq application.
- **Scope application** – This software is shipped with the board on the Data Acquisition OMNI CD. This application emulates three basic instruments: a simple oscilloscope chart recorder, a data logger, and a multi-channel oscilloscope. Using the Scope application, you can monitor data online and capture it to disk. Refer to the online documentation provided on the CD-ROM for more information.
- **DT3010 and DT3016 Calibration Utilities** – This software is shipped with the board on the Data Acquisition OMNI CD. The DT3010 Calibration Utility allows you to calibrate the analog input and analog output subsystems of the DT3010, DT3010-268, DT3010/32, and DT3010/32-268 boards. The DT3016 Calibration Utility allows you to calibrate the analog input and analog output subsystems of the DT3016 board. Refer to page 125 for more information on these utilities.

- **DT Measure Foundry** – An evaluation version of this software is included on the Data Acquisition OMNI CD. DT Measure Foundry is drag-and-drop test and measurement application builder designed to give you top performance with ease-of-use development. Order the full development version of this software package to develop your own application using real hardware.
- **DataAcq SDK** – This software is shipped on the Data Acquisition OMNI CD. Use the Data Acq SDK if you want to use Windows 98, Windows Me, Windows NT 4.0, Windows 2000, or Windows XP to develop your own application software for the DT3010 Series boards using the Microsoft C compiler; the DataAcq SDK complies with the DT-Open Layers standard.
- **DTx-EZ** – Order this optional software package if you want to use ActiveX controls to access the capabilities of the DT3010 Series boards using Microsoft Visual Basic or Visual C++; DTx-EZ complies with the DT-Open Layers standard.
- **DT VPI** – Order this optional software package if you want to use the Aglient VEE visual programming language to access the capabilities of the DT3010 Series boards.
- **DT-LV Link** – Order this optional software package if you want to use the LabVIEW graphical programming language to access the capabilities of the DT3010 Series boards.
- **Testpoint** – Order this optional software package if you want use a drag-and-drop software environment for designing test, measurement, and data acquisition applications.

Refer to the catalog to determine the appropriate software package for your application.

Accessories

The following optional accessories are available for DT3010 Series boards:

- **DT740 screw terminal panel** – Screw terminal panel with two connectors to accommodate the analog I/O, digital I/O, and counter/timer signals provided by the DT3010, DT3010/32, DT3010/32-268, and DT3016 boards.
- **EP307 cable** – A 1-meter, twisted-pair, shielded cable that connects the 50-pin analog I/O connector (J1) on the DT3010, DT3010/32, DT3010/32-268, and DT3016 boards to the J1 connector on the DT740 screw terminal panel.
- **EP308 cable** – A 1-meter, twisted-pair, shielded cable that connects the 68-pin digital I/O connector (J2) on the DT3010, DT3010/32, DT3010/32-268, and DT3016 boards to the J2 connector on the DT740 screw terminal panel.
- **STP268 screw terminal panel** – Screw terminal panel with one 68-pin connector to access the signals provided by one of the connectors on the DT3010-268 board. If you want to access all of the functionality of the DT3010-268 at the same time, you need two STP268 screw terminal panels.
- **STP268-EC screw terminal panel** – Screw terminal panel with two 26-pin connectors for attaching to 5B or 7B Series signal conditioning backplanes, one 50-pin connector for attaching to the Opto-22 PB16H backplane, and one 68-pin connector for attaching to the DT3010-268 board.
- **EP324 cable** – A 1 1/2-inch ribbon cable that connects to the 68-pin digital I/O connector (J2) on the DT3010-268 board; the other end of this cable provides a 68-pin connector and face plate for connection to an EP325 cable. This cable is shipped with each DT3010-268 board.
- **EP325 cable** – A, 6-foot, SCSI-3 cable that connects the STP268 or STP268-EC screw terminal panel to connector J1 on the DT3010-268 board.

- **5B01** – a 16-channel backplane that accepts 5B Series signal conditioning modules.
- **5B08** – an 8-channel backplane that accepts 5B Series signal conditioning modules.
- **7BP16-1** – a 16-channel backplane that accepts 7B Series signal conditioning modules.
- **7BP08-1** – an 8-channel backplane that accepts 7B Series signal conditioning modules.
- **7BP04-1** – a 4-channel backplane that accepts 7B Series signal conditioning modules.
- **PB16H** – a digital backplane that connects to the STP268-EC screw terminal panel to allow access to digital I/O signals.
- **AC1315** – a 2-foot, 26-pin female to 26-pin female cable that connects a 5B Series backplane to an STP268-EC screw terminal panel.
- **AC1393** – a 6-inch, 26-pin male to 25-pin female adapter cable that connects a 7B Series backplane to the AC1315 cable; the AC1315 cable then connects to an STP268-EC screw terminal panel.
- **EP035** – a 2.4-meter, 50-pin ribbon cable that connects the PB16H Opto 22 backplane to an STP268-EC screw terminal panel.

2

Principles of Operation

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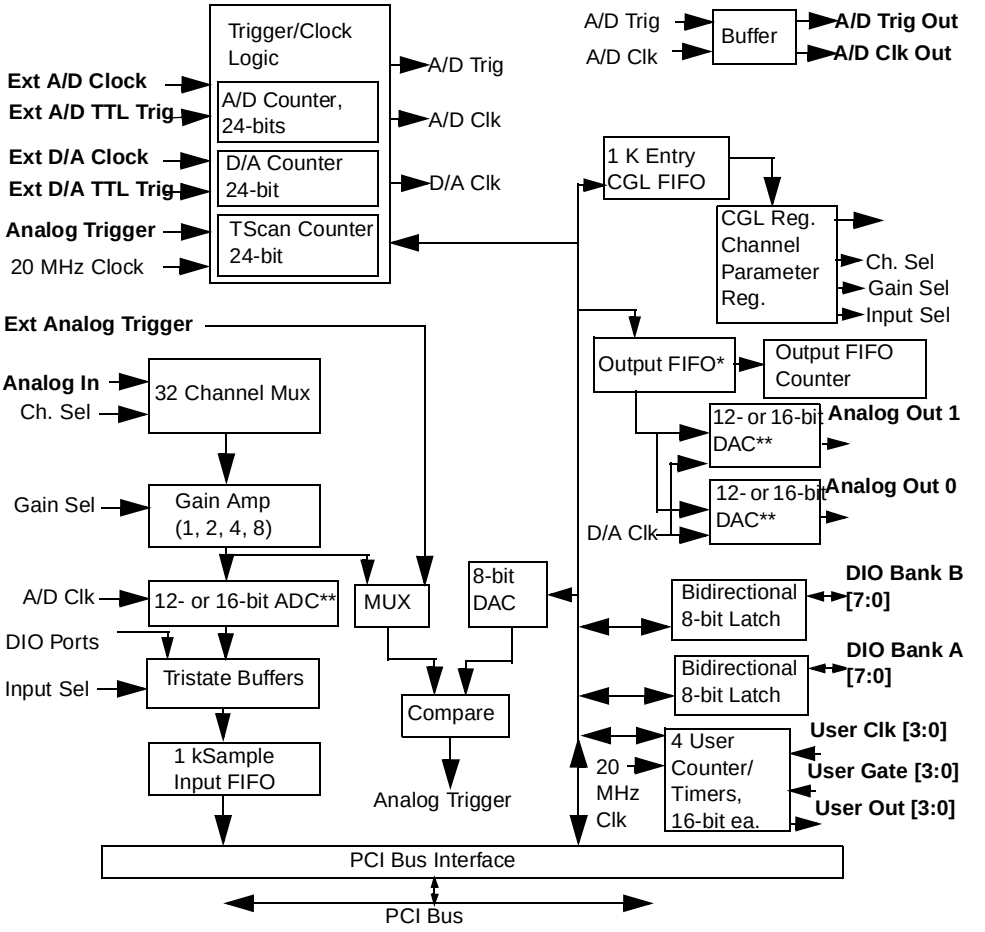
This chapter describes the analog input, analog output, digital I/O, counter/timer, and synchronous features of the DT3010 Series boards. To frame the discussions, refer to the block diagram shown in Figure 1. Note that bold entries indicate signals you can access.



*The DT3010, DT3010-268, and DT3016 have a 4 kSample output FIFO; the DT3010/32 and DT3010/32-268 have a 32 kSample output FIFO.**Only the DT3016 has a 16-bit ADC and 16-bit DACs.

Figure 1: Block Diagram of the DT3010 Series Boards

Analog Input Features

This section describes the features of the analog input (A/D) subsystem, including the following:

- Analog input resolution,
- Analog input channels,
- Input ranges and gains,
- A/D sample clock sources,
- Analog input conversion modes,
- Trigger sources and trigger acquisition modes,
- Data formats and transfer, and
- Error conditions.

Analog Input Resolution

DT3010, DT3010-268, DT3010/32, and DT3010/32-268 boards have a fixed analog input resolution of 12 bits. The DT3016 board has a fixed resolution of 16 bits. The analog input resolution cannot be changed in software.

Analog Input Channels

DT3010 Series boards support 32 single-ended or pseudo-differential analog input channels, or 16 differential analog input channels. Refer to the *DT3010 Series Getting Started Manual* for a description of how to wire these signals. Use software to specify the channel type.

Note: For pseudo-differential inputs, specify single-ended in software; in this case, how you wire these signals determines the configuration.

DT3010 Series boards can acquire data from a single analog input channel or from a group of analog input channels. Channels are numbered 0 to 31 for single-ended and pseudo-differential inputs, and 0 to 15 for differential inputs. The following subsections describe how to specify the channels.

Specifying a Single Channel

The simplest way to acquire data from a single channel is to specify the channel for a single-value analog input operation using software; refer to page 20 for more information on single-value operations.

You can also specify a single channel using the analog input channel list, described in the next section.

Specifying One or More Channels

DT3010 Series boards can read data from one or more analog input channels using an analog input channel list. You can group the channels in the list sequentially (either starting with 0 or with any other analog input channel), or randomly. You can also specify a single channel or the same channel more than once in the list.

Using software, specify the channels in the order you want to sample them. The analog input channel list corresponds to the Channel-Gain List FIFO on the board. You can enter up to 1,024 entries. The channels are read in order (using continuously- paced scan mode or triggered scan mode) from the first entry to the last entry in the channel list. The board can read the channels in the channel list up to 256 times per trigger (for a total of 262,144 samples per trigger) using

triggered scan mode. Refer to page 20 for more information on the supported conversion modes.

If you wish, you can also use software to set up a channel-inhibit list. This feature is useful if you want to discard acquired values from specific entries in the channel list. Using the channel-inhibit list, you can enable or disable inhibition for each entry in the analog input channel list. If enabled, the value is discarded after the channel is read; if disabled, the value is not discarded after the channel is read.

Note: If you select an analog input channel as the analog threshold trigger source, the channel used for this trigger source must be the first channel specified in the analog input channel list; refer to page 28 for more information on this trigger source.

Specifying Digital Input Lines in the Analog Input Channel List

In addition to the analog input channels, you can read the 16 digital I/O lines (Bank A 0 to 7 and Bank B 0 to 7) of the DT3010 Series boards using the analog input channel list. This feature is particularly useful when you want to correlate the timing of analog and digital events.

To read these 16 digital I/O lines, specify channel 32 in the analog input channel list. You can enter channel 32 anywhere in the list and can enter it more than once, if desired.

This channel is treated like any other channel in the analog input channel list; therefore, all the clocking, triggering, and conversion modes supported for analog input channels are supported for these digital I/O lines, if you specify them in this manner.

Performing Dynamic Digital Output Operations

Using software, you can enable a synchronous dynamic digital output operation for the A/D subsystem. This feature is particularly useful for synchronizing and controlling external equipment.

Two dynamic digital output lines are provided: 0 and 1. These lines are set to a value of 0 on power up; a reset does not affect the values of the dynamic digital output lines. Note that these lines are provided in addition to the other 16 digital I/O lines; see page 52 for more information on the digital I/O features.

Using software, specify the values to write to the dynamic digital output lines using the analog input channel list. As each entry in the analog input channel list is read, the corresponding value you specified is output to the dynamic digital output lines.

For DT3010 Series boards, you can specify the following values for the dynamic digital output lines: 0 (00 in binary format), 1 (01 in binary format), 2 (10 in binary format), or 3 (11 in binary format), where a value of 1 means that the line goes high and a value of 0 means that the line goes low. Each bit in binary format corresponds to the value to write to the dynamic digital output line. For example, a value of 1 (01 in binary format) means that a value of 1 is output to dynamic digital output line 0 and value of 0 is output to dynamic output line 1. Similarly, a value of 2 (10 in binary format) means that a value of 0 is output to dynamic digital output line 0 and value of 1 is output to dynamic output line 1.

For example, assume that the analog input channel list contains channels 5, 6, 7, 8; that dynamic digital output operations are enabled; and that the values to write to the dynamic digital output lines are 2, 0, 1, 3. Figure 2 shows this configuration.

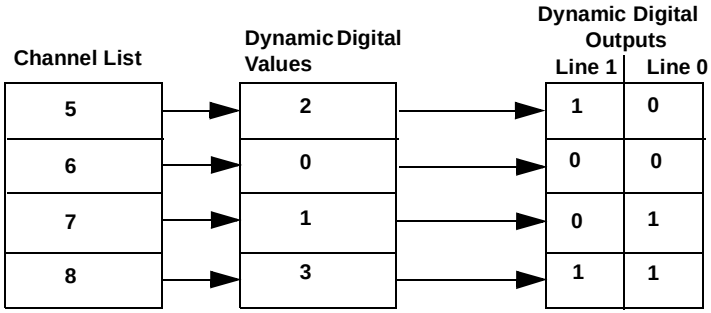


Figure 2: An Example Using Dynamic Digital Outputs

As analog input channel 5 is read, 1 is output to dynamic digital output line 1, and 0 is output to dynamic output line 0 (since 2 in binary format is 10). As analog input channel 6 is read, 0 is output to both dynamic digital output lines. As analog input channel 7 is read, 0 is output to dynamic digital output line 1, and 1 is output to dynamic output line 0 (since 1 in binary format is 01). As analog input channel 8 is read, 1 is written to both dynamic digital output lines.

Input Ranges and Gains

Each channel on the DT3010 Series board can measure unipolar and bipolar analog input signals. A unipolar signal is always positive (0 to 10 V on DT3010 Series boards), while a bipolar signal extends between the negative and positive peak values (±10 V on DT3010 Series boards).

Through software, specify the range as 0 to 10 V for unipolar signals or –10 V to +10 V for bipolar signals. Note that the range applies to the entire analog input subsystem, not to a specific channel.

DT3010 Series boards also provide gains 1, 2, 4, and 8, which are programmable per channel. Table 2 lists the effective ranges supported by DT3010 Series boards using these gains.

Table 2: Gains and Effective Ranges

Gain	Unipolar Analog Input Range	Bipolar Analog Input Range
1	0 to 10 V	±10 V
2	0 to 5 V	±5 V
4	0 to 2.5 V	±2.5 V
8	0 to 1.25 V	±1.25 V

For each channel, choose the gain that has the smallest effective range that includes the signal you want to measure. For example, if the range of your analog input signal is ±1.5V, specify a range of –10 V to +10 V for the board and use a gain of 4 for the channel; the effective input range for this channel is then ±2.5V, which provides the best sampling accuracy for that channel.

The way you specify gain depends on how you specified the channels, as described in the following subsections.

Specifying the Gain for a Single Channel

The simplest way to specify gain for a single channel is to specify the gain for a single-value analog input operation using software; refer to page 20 for more information on single-value operations.

You can also specify the gain for a single channel using an analog input gain list, described in the next section.

Specifying the Gain for One or More Channels

On the DT3010 Series, you can specify the gain for one or more analog input channels using an analog input gain list. Using software, set up the gain list by specifying the gain for each entry in the analog input channel-gain list. The gain list parallels the channel list. (The two lists together are often referred to as the channel-gain list.)

For example, assume the analog input channel list contains three entries: channels 5, 6, and 7; the gain list might look like this: 2, 4, 1, where a gain of 2 corresponds to channel 5, a gain of 4 corresponds to channel 6, and a gain of 1 corresponds to channel 7.

Note: For analog input channel 32 (the 16 digital I/O channels) in the channel list, specify a gain of 1 in the gain list.

A/D Sample Clock Sources

DT3010 Series boards provide two clock sources for pacing analog input operations in continuous mode:

- An internal A/D sample clock that uses the 24-bit A/D Counter on the board, and
- An external A/D sample clock that you can connect to the screw terminal panel.

The A/D sample clock paces the acquisition of each channel in the channel-gain list; this clock is also called the A/D pacer clock.

Note: If you enter digital I/O channel 32 in the channel-gain list, the A/D sample clock (internal or external) also paces the acquisition of the 16 digital input lines.

The following subsections describe the internal and external A/D sample clocks in more detail.

Internal A/D Sample Clock

The internal A/D sample clock uses a 20 MHz time base. Conversions start on the falling edge of the counter output; the output pulse is active low.

Using software, specify the clock source as internal and the clock frequency at which to pace the operation. The minimum frequency supported is 1.2 Hz (1.2 Samples/s). For the DT3010, DT3010-268, DT3010/32, and DT3010/32-268 boards, the maximum frequency supported is 1.25 MHz (1.25 MSamples/s). For the DT3016 board, the maximum frequency supported is 250 kHz (250 kSamples/s).

According to sampling theory (Nyquist Theorem), specify a frequency that is at least twice as fast as the input's highest frequency component. For example, to accurately sample a 20 kHz signal, specify a sampling frequency of at least 40 kHz. Doing so avoids an error condition called *aliasing*, in which high frequency input components erroneously appear as lower frequencies after sampling.

Note: You can access the output signal from the A/D sample clock using screw terminal 79 on the DT740 screw terminal panel, or screw terminal 47 on the STP268 screw terminal panel (attached to connector J1) or STP268-EC screw terminal panel.

External A/D Sample Clock

The external A / D sample clock is useful when you want to pace acquisitions at rates not available with the internal A / D sample clock or when you want to pace at uneven intervals.

Connect an external A / D sample clock to screw terminal 76 on the DT740 screw terminal panel, screw terminal 48 on the STP268 screw terminal panel (attached to connector J1), or screw terminal 13 on the STP268-EC screw terminal panel. Conversions start on the falling edge of the external A / D sample clock input signal.

Using software, specify the clock source as external. For DT3010 Series boards, the clock frequency is always equal to the frequency of the external A / D sample clock input signal that you connect to the board through the screw terminal panel.

Note: The DT3010-268 board only provides an External A / D Trigger and Clock Enable signal. This signal is pulled high on the DT3010-268 board by a 22 kΩ resistor. You can use this signal to enable or disable the external digital trigger and the external A / D sample clock.

A high signal enables both the external digital trigger and the external A / D sample clock, while a low signal disables both the external digital trigger and the external A / D sample clock.

Analog Input Conversion Modes

DT3010 Series boards support the following conversion modes:

- **Single-value operations** are the simplest to use but offer the least flexibility and efficiency. Use software to specify the range, gain, and analog input channel (among other parameters); acquire the data from that channel; and convert the result. The data is returned immediately. For a single-value operation, you cannot specify a clock source, trigger source, trigger acquisition mode, scan mode, or buffer.

  Single-value operations stop automatically when finished; you cannot stop a single-value operation.

- **Scan mode** takes full advantage of the capabilities of the DT3010 Series boards. In a scan, you can specify a channel-gain list, clock source, trigger source, trigger acquisition mode, scan mode, buffer, and buffer wrap mode. Two scan modes are supported: continuously-paced scan mode and triggered scan mode (often called burst mode). These modes are described in the following subsections.

  Using software, you can stop a scan mode operation by performing either an orderly stop or an abrupt stop. In an orderly stop, the board finishes acquiring the specified number of samples, stops all subsequent acquisition, and transfers the acquired data to host memory; all subsequent triggers or retriggers are ignored. In an abrupt stop, the board stops acquiring samples immediately; the acquired data is not transferred to host memory, but all subsequent triggers or retriggers are ignored.

Continuously-Paced Scan Mode

Use continuously-paced scan mode if you want to accurately control the period between conversions of individual channels in a scan.

When it detects an initial trigger, the board cycles through the channel-gain list, acquiring and converting the value for each entry in the channel list; this process is defined as the scan. The board then wraps to the start of the channel-gain list and repeats the process continuously until either the allocated buffers are filled or you stop the operation. Refer to page 36 for more information on buffers.

The conversion rate is determined by the frequency of the A/D sample clock; refer to page 17 for more information on the A/D sample clock. The sample rate, which is the rate at which a single entry in the channel-gain list is sampled, is determined by the frequency of the A/D sample clock divided by the number of entries in the channel-gain list.

To select continuously-paced scan mode, use software to specify the dataflow as continuous, continuous pre-trigger, or continuous about-trigger; refer to page 29 for more information about these trigger acquisition modes.

The initial trigger source depends on the trigger acquisition mode selected; refer to page 26 for more information on the supported trigger acquisition modes and trigger sources.

Note: An A/D Trigger Out signal is provided for your use. This signal is high when the A/D subsystem is waiting for a trigger and low when a trigger occurs. In continuously-paced scan mode, this signal goes low when the trigger occurs and stays low until you stop the operation.

Triggered Scan Mode

DT3010 Series boards support two triggered scan modes: internally-retriggered and externally-retriggered. These modes are described in the following subsections.

Internally-Retriggered Scan Mode

Use internally-retriggered scan mode if you want to accurately control both the period between conversions of individual channels in a scan and the period between each scan. This mode is useful when synchronizing or controlling external equipment, or when acquiring a buffer of data on each trigger or retrigger. Using this mode, you can acquire up to 262,144 samples per trigger (256 times per trigger x 1024-location channel-gain list).

When it detects an initial trigger, the board scans the channel-gain list a specified number of times (up to 256), then waits for an internal retrigger to occur. When the board detects an internal retrigger, the board scans the channel-gain list the specified number of times, then waits for another internal retrigger to occur. The process repeats continuously until either the allocated buffers are filled or you stop the operation; refer to page 36 for more information on buffers.

The sample rate is determined by the frequency of the A/D sample clock divided by the number of entries in the channel-gain list; refer to page 17 for more information on the A/D sample clock. The conversion rate of each scan is determined by the frequency of the internal retrigger clock. The internal retrigger clock is the Triggered Scan Counter, a 24-bit counter with a 20MHz clock located on the board.

Using software, specify the frequency of the internal retrigger clock. The minimum retrigger frequency is 1.2 Hz. For DT3010, DT3010-268, DT3010/32, and DT3010/32-268 boards, the maximum retrigger frequency is 357.14 kHz (357.14 kSamples/s); for DT3016 boards, the maximum retrigger frequency is 166.67 kHz (166.666 kSamples/s).

Specify the *retrigger frequency* as follows:

$$\text{Min. Retrigger Period} = \frac{\text{\# of CGL entries x \# of CGLs per trigger}}{\text{A/D sample clock frequency}} + 2\ \mu s$$

$$\text{Max. Retrigger Frequency} = \frac{1}{\text{Min. Retrigger Period}}$$

For example, if you are using 512 channels in the channel-gain list (CGL), scanning the channel-gain list 256 times every trigger or retrigger, and using an A/D sample clock with a frequency of 1 MHz, set the maximum retrigger frequency to 7.62 Hz, since

$$7.62\ \text{Hz} = \frac{1}{\frac{(512 * 256)}{1\ \text{MHz}} + 2\ \mu s}$$

To select internally-retriggered scan mode, use software to specify the following parameters:

- The dataflow as continuous, continuous pre-trigger, or continuous about-trigger,
- Triggered scan mode usage as enabled,
- The retrigger mode as internal,
- The number of times to scan per trigger or retrigger (also called the multiscan count), and
- The frequency of the retrigger clock.

The initial trigger source depends on the trigger acquisition mode selected; refer to page 26 for more information on the supported trigger acquisition modes and trigger sources.

Note: An A/D Trigger Out signal is provided for your use. This signal is high when the A/D subsystem is waiting for a trigger and low when a trigger occurs. In internally-retriggered scan mode, this signal stays low until the desired number of samples have been acquired, then goes high until the internal retrigger is generated.

Externally-Retriggered Scan Mode

Use externally-retriggered scan mode if you want to accurately control the period between conversions of individual channels and retrigger the scan based on an external event. Like internally-retriggered scan mode, this mode allows you to acquire 262,144 samples per trigger (256 times per trigger x 1024-location channel-gain list).

Note: Use externally-retriggered scan mode with continuous post-trigger acquisitions only; refer to page 29 for more information on post-trigger acquisitions.

When it detects an initial trigger (post-trigger source only), the board scans the channel-gain list up to 256 times, then waits for an external retrigger to occur. Specify any supported post-trigger source as the initial trigger. For the retrigger, specify either an external digital (TTL) trigger or an external analog threshold trigger.

When the retrigger occurs, the board scans the channel-gain list the specified number of times, then waits for another external retrigger to occur. The process repeats continuously until either the allocated buffers are filled or you stop the operation; refer to page 36 for more information on buffers.

The conversion rate of each channel is determined by the frequency of the A / D sample clock; refer to page 17 for more information on the A / D sample clock. The conversion rate of each scan is determined by the period between external retriggers; therefore, it cannot be accurately controlled. The board ignores external triggers that occur while it is acquiring data. Only external retrigger events that occur when the board is waiting for a retrigger are detected and acted on.

To select externally-retriggered scan mode, use software to specify the following parameters:

- The dataflow as continuous (post-trigger),
- Triggered scan mode as enabled,
- The retrigger mode as an external retrigger (retrigger extra for DataAcq SDK users),
- The number of times to scan per trigger or retrigger (also called the multiscan count), and
- The retrigger source as the external digital (TTL) trigger or an external analog threshold trigger.

Note: If you are using an external trigger source as the initial trigger and want to retrigger externally, specify the same trigger source as the retrigger. For example, if you are using an external digital (TTL) trigger as the initial trigger, specify the external digital (TTL) trigger as the retrigger.

Notes: An A/D Trigger Out signal is provided for your use. This signal is high when the A/D subsystem is waiting for a trigger and low when a trigger occurs. In externally-retriggered scan mode, this signal stays goes low when the trigger occurs and stays low until the desired number of samples have been acquired, then goes high until the external retrigger is generated.

For DataAcq SDK users, if you want to use the same trigger source as both the initial trigger and the retrigger source, specify the retrigger mode as scan-per-trigger. In this case, you need not specify the retrigger source; the board uses the initial post-trigger source as the retrigger source. Ensure that you specify the external digital (TTL) trigger or an external analog threshold trigger as the initial trigger source.

Triggers

A trigger is an event that occurs based on a specified set of conditions. DT3010 Series boards support a number of trigger sources and trigger acquisition modes, described in the following subsections.

Trigger Sources

DT3010 Series boards support the following trigger sources:

- Software trigger,
- External digital (TTL) trigger, and
- Analog threshold trigger.

This subsection describes these trigger sources in more detail.

Software Trigger

A software trigger event occurs when you start the analog input operation (the computer issues a write to the board to begin conversions). Specify the software trigger source in software.

External Digital (TTL) Trigger

For analog input operations, an external digital trigger event occurs when the DT3010 Series board detects either a rising or falling edge on the External A / D TTL Trigger input signal connected to screw terminal 77 on the DT740 screw terminal panel, screw terminal 49 on the STP268 screw terminal panel (attached to connector J1), or screw terminal 14 on the STP268-EC screw terminal panel. The trigger signal is TTL-compatible.

Using software, specify the trigger source as a rising-edge external digital trigger (external for DataAcq SDK users) or a falling-edge external digital trigger (extra for DataAcq SDK users).

Note: The DT3010-268 board only provides an External A / D Trigger and Clock Enable signal. This signal is pulled high on the DT3010-268 board by a 22 kΩ resistor. You can use this signal to enable or disable the external digital trigger and the external A / D sample clock.

A high signal enables both the external digital trigger and the external A / D sample clock, while a low signal disables both the external digital trigger and the external A / D sample clock.

Analog Threshold Trigger

For analog input operations, an analog trigger event occurs when the DT3010 Series detects a transition from above a threshold level to below a threshold level (falling edge), or a transition from below a threshold level to above a threshold level (rising edge). The following analog threshold trigger sources are available:

- **External Analog Trigger input signal** connected to screw terminal 107 on the DT740 screw terminal panel, screw terminal 39 on the STP268 screw terminal panel (attached to connector J1), or screw terminal 15 on the STP268-EC screw terminal panel. Using software, specify the trigger source as either a rising-edge (extra+1 for DataAcq SDK users) or falling-edge analog threshold trigger (extra +2 for DataAcq SDK users)
- **One of the analog input channels** after gain is applied (also called the output of the programmable gain amplifier (PGA)**.** Using software, specify the trigger source as either a positive threshold trigger or negative threshold trigger.
  Using software, specify the analog input channel used as the analog threshold trigger as the first channel in the channel list; refer to page 12 for more information.

On DT3010 Series boards, the threshold level is set using a dedicated 8-bit DAC; the hysteresis is fixed at 50 mV. Using software, program the threshold level by writing a voltage value to this DAC; this value can range from –10 V to +10 V.

Note: If you are using an analog threshold trigger to trigger both the A / D and the D / A subsystems, ensure that you use the same analog trigger type for both subsystems (either external or one of the analog input channels). The polarity of the triggers, however, can be different.

Trigger Acquisition Modes

DT3010 Series boards can acquire data in post-trigger mode, pre-trigger mode, or about-trigger mode. These trigger acquisition modes are described in more detail in the following subsections.

Post-Trigger Acquisition

Use post-trigger acquisition mode (continuous mode) when you want to acquire data when a post-trigger or retrigger, if using triggered scan mode, occurs.

Using software, specify the following parameters:

- The dataflow as continuous, and
- The trigger source to start the post-trigger acquisition (the post-trigger source) as any of the supported trigger sources.

Refer to page 20 for more information on the supported conversion modes; refer to page 26 for information on the supported trigger sources.

Post-trigger acquisition starts when the board detects the post-trigger event and stops when the specified number of post-trigger samples has been acquired (if the buffer wrap mode is none, described on page 38), or when you stop the operation.

If you are using triggered scan mode, the board continues to acquire post-trigger data using the specified retrigger source to clock the operation. Refer to page 22 for more information on triggered scan mode.

Figure 3 illustrates continuous post-trigger mode using a channel-gain list with three entries: channel 0, channel 1, and channel 2. Triggered scan mode is disabled. In this example, post-trigger analog input data is acquired on each clock pulse of the A/D sample clock. The board wraps to the beginning of the channel-gain list and repeats continuously (continuously-paced scan mode).

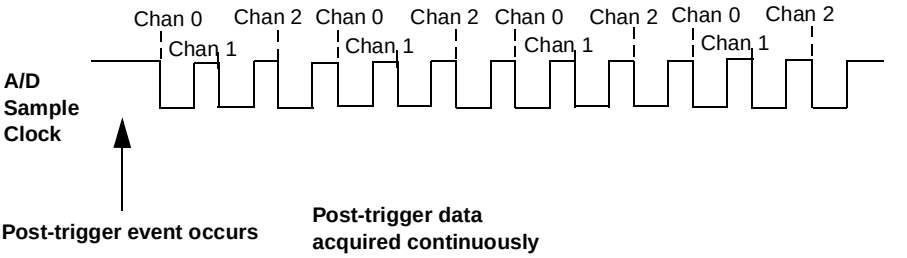


Figure 3: Continuous Post-Trigger Mode without Triggered Scan

Figure 4 illustrates the same example using triggered scan mode (either internally- or externally-retriggered). The multiscan count is 2 indicating that the channel-gain list will be scanned twice per trigger or retrigger. In this example, post-trigger analog input data is acquired on each clock pulse of the A/D sample clock until the channel-gain list has been scanned twice; then, the board waits for the retrigger event. When the retrigger event occurs, the board scans the channel-gain list twice more, acquiring data on each pulse of the A/D sample clock. The process repeats continuously with every specified retrigger event.

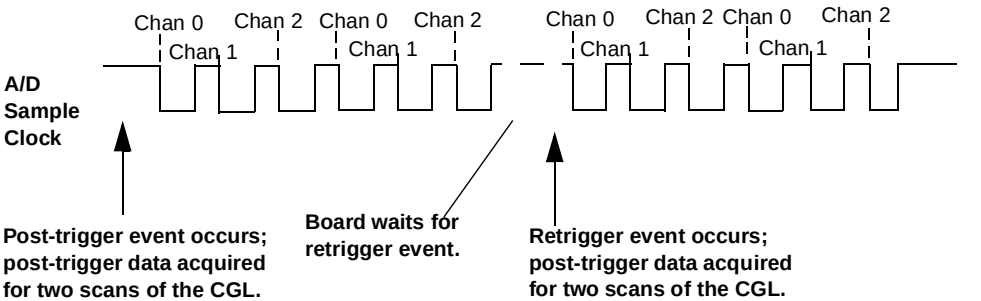


Figure 4: Continuous Post-Trigger Mode with Triggered Scan

Pre-Trigger Acquisition

Use pre-trigger acquisition mode (continuous pre-trigger mode) when you want to acquire data before a specific external event occurs.

Using software, specify the following parameters:

- The dataflow as continuous pre-trigger,
- The pre-trigger source as the software trigger,
- The post-trigger source as the external digital (TTL) trigger or the external analog threshold trigger, and
- If you are using triggered scan mode, the retrigger mode as the internal retrigger.

Refer to page 20 for more information on the supported conversion modes; refer to page 26 for information on the supported trigger sources.

Note: When using pre-trigger acquisition, you cannot use an external retrigger in triggered scan mode; refer to page 22 for more information on triggered scan mode.

Pre-trigger acquisition starts when you start the operation and stops when the board detects the selected post-trigger source, indicating that the first post-trigger sample was acquired (this sample is ignored).

If you are using internally-retriggered scan mode and the post-trigger event has not occurred, the board continues to acquire pre-trigger data using the internal retrigger clock to clock the operation. When the post-trigger event occurs, the operation stops. Refer to page 22 for more information on internally-retriggered scan mode.

Figure 5 illustrates continuous pre-trigger mode using a channel-gain list of three entries: channel 0, channel 1, and channel 2. In this example, pre-trigger analog input data is acquired on each clock pulse of the A / D sample clock. The board wraps to the beginning of the channel-gain list and the acquisition repeats continuously until the post-trigger event occurs. When the post-trigger event occurs, acquisition stops.

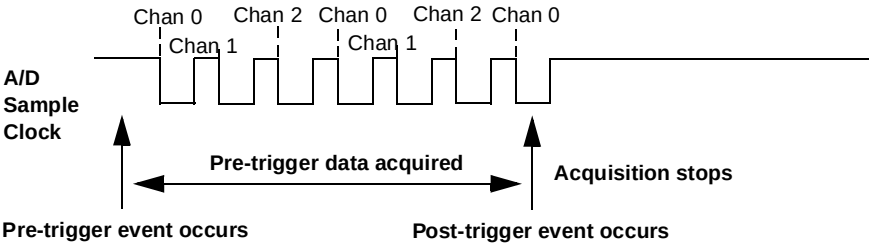


Figure 5: Continuous Pre-Trigger Mode

Figure 6 illustrates the same example using internally-retriggered triggered scan mode. The multiscan count is 2 indicating that the channel-gain list will be scanned twice per trigger or retrigger. In this example, pre-trigger analog input data is acquired on each clock pulse of the A / D sample clock until the channel-gain list has been scanned twice; then, the board waits for the internal retrigger event. When the internal retrigger occurs, the process repeats. The process stops when the post-trigger event occurs.

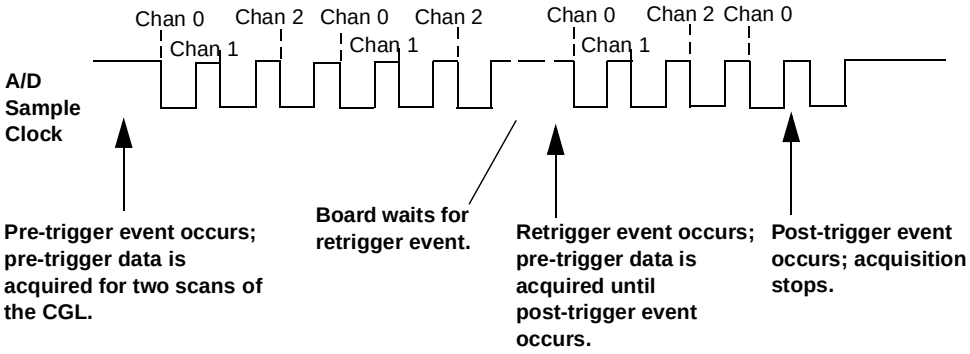


Figure 6: Continuous Pre-Trigger Mode with Triggered Scan

About-Trigger Acquisition

Use about-trigger acquisition mode (continuous about-trigger mode) when you want to acquire data both before and after a specific external event occurs. This operation is equivalent to doing both a pre-trigger and a post-trigger acquisition.

Using software, specify the following parameters:

- The dataflow as continuous about-trigger,
- The pre-trigger source as the software trigger,
- The post-trigger source as the external digital (TTL) trigger or the external analog threshold trigger, and
- If you are using triggered scan mode, the retrigger mode as the internal retrigger.

Refer to page 20 for more information on the supported conversion modes; refer to page 26 for information on the supported trigger sources.

Note: When using about-trigger acquisition, you cannot use an external retrigger in triggered scan mode; refer to page 22 for more information on triggered scan mode.

The about-trigger acquisition starts when you start the operation. When the board detects the selected post-trigger event, the board stops acquiring pre-trigger data and starts acquiring post-trigger data.

If you are using internally-retriggered scan mode and the post-trigger event has not occurred, the board continues to acquire pre-trigger data using the internal retrigger clock to clock the operation. If, however, the post-trigger event has occurred, the board continues to acquire post-trigger data using the internal retrigger clock to clock the operation.

The about-trigger operation stops when the specified number of post-trigger samples has been acquired (if the buffer wrap mode is none, described on page 38), or when you stop the operation. Refer to page 22 for more information on internally-retriggered scan mode.

Figure 7 illustrates continuous about-trigger mode using a channel list of two entries: channel 0 and channel 1. In this example, pre-trigger analog input data is acquired on each clock pulse of the A/D sample clock, scanning the channel list continuously, until the post-trigger event occurs. When the post-trigger event occurs, post-trigger analog input data is acquired continuously on each clock pulse of the A/D sample clock.

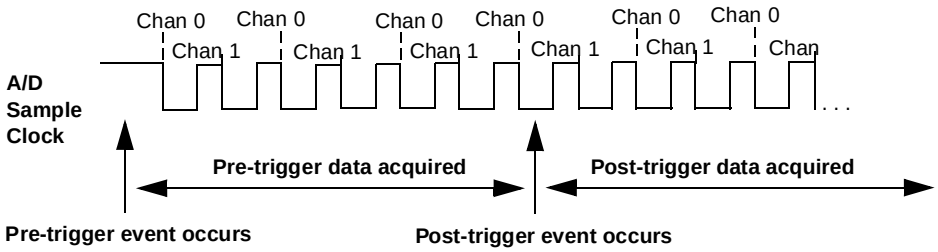


Figure 7: Continuous About-Trigger Mode

Figure 8 illustrates the same example using internally-retriggered triggered scan mode. The multiscan count is 2 indicating that the channel-gain list will be scanned twice per trigger or retrigger. In this example, pre-trigger analog input data is acquired on each clock pulse of the A / D sample clock for two scans; then, the board waits for the internal retrigger event. When the internal retrigger occurs, the board begins acquiring pre-trigger data until the post-trigger event occurs. Then, the board finishes scanning the channel-gain list the specified number of times, but acquires the data as post-trigger samples. On all subsequent internal retriggers, post-trigger data is acquired.

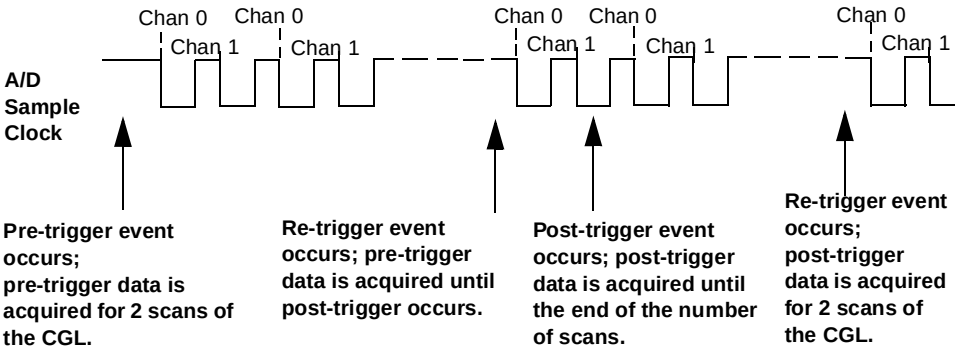

Chan 0
Chan 1
Chan 0
Chan 1
Chan 0
Chan 1
Chan 0
Chan 1
Chan 0
Chan 1
A/D
Sample
Clock
Pre-trigger event occurs; pre-trigger data is acquired for 2 scans of the CGL.
Re-trigger event occurs; pre-trigger data is acquired until post-trigger occurs.
Post-trigger event occurs; post-trigger data is acquired until the end of the number of scans.
Re-trigger event occurs; post-trigger data is acquired for 2 scans of the CGL.

Figure 8: Continuous About-Trigger Mode with Triggered Scan

Data Format and Transfer

To represent unipolar signals, DT3010 Series boards use straight binary data encoding, such as 000 (for 12-bit boards) or 0000 (for 16-bit boards) to represent 0 V, and FFFh (for 12-bit boards) or FFFFh (for 16-bit boards) to represent full-scale. To represent bipolar signals, DT3010 Series boards use offset binary data encoding, such as 000 (for 12-bit boards) or 0000 (for 16-bit boards) to represent negative full-scale, and FFFh (for 12-bit boards) or FFFFh (for 16-bit boards) to represent positive full-scale. Use software to specify the data encoding as binary.

The ADC outputs FFFh (for 12-bit boards) or FFFFh (for 16-bit boards) for above-range signals, and 000 (for 12-bit boards) or 0000 (for 16-bit boards) for below-range signals.

The board packs two input samples (an even and an odd sample) into each transfer to the host computer. Samples corresponding to entries 0, 2, 4, and so on, in the channel-gain list are considered even samples; samples corresponding to entries 1, 3, 5, and so on, in the channel-gain list are considered odd samples.

Using flags internally, the board determines whether the acquired samples are pre-trigger or post-trigger samples. These flags are not transferred to the host computer. The host computer can read the register on the board to determine where the post-trigger data starts. Note that the host computer cannot read data directly from the board; the data must be transferred to the host computer. Unlike ISA and EISA boards, DT3010 Series boards require no DMA resources since they use PCI bus mastering to transfer data from the board to the host computer.

Using PCI bus mastering, the board transfers the analog input data to a 256 KB circular buffer, which is dedicated to the hardware, in the host computer. The board treats this buffer as two consecutive 128 KB blocks of memory.

Note: When you stop an analog input operation, a final block of 32 samples is transferred even if less data is required. The host software ignores the extra samples.

The DT3010 Series Device Driver accesses the hardware circular buffer to fill user buffers that you allocate in software. It is recommended that you allocate a minimum of three buffers for analog input operations, specifying one of the following buffer wrap modes in software:

- **None** – If the wrap mode is none (for gap-free data), data is written to the allocated buffers until no more empty buffers are available; then, the operation stops.
- **Multiple** – If wrap mode is multiple, data is written to the allocated multiple buffers continuously; when no more empty buffers are available, the board overwrites the data in the filled buffers starting with the first location of the first buffer. This process continues indefinitely until you stop it.
- **Single** – If wrap mode is single, data is written to a single buffer continuously; when the buffer is filled, the board overwrites the data in the buffer starting with the first location of the buffer. This process continues indefinitely until you stop it.

Error Conditions

DT3010 Series boards can report the following analog input error conditions to the host computer:

- **A/D Over Sample** - Indicates that the A/D sample clock rate is too fast. This error is reported if a new A/D sample clock pulse occurs while the ADC is busy performing a conversion from the previous A/D sample clock pulse. The host computer can clear this error. To avoid this error, use a slower sampling rate.

- **Input FIFO Overflow** - Indicates that the analog input data is not being transferred fast enough from the Input FIFO across the PCI bus to the host computer. This error is reported when the Input FIFO becomes full; the board cannot get access to the PCI bus fast enough. The host computer can clear this error, but the error will continue to be generated if the Input FIFO is still full. To avoid this error, close other applications that may be running while you are acquiring data. If this has no effect, try using a computer with a faster processor or reduce the sampling rate.
- **Host Block Overflow** - Indicates that the host computer is not handling data from the board fast enough. This error is reported if the board completes the transfer of a block of input data to the circular buffer in the host computer before the host computer has finished reading the last block of data. The host computer can clear this error. To avoid this error, ensure that you allocated at least three buffers at least as large as the sampling rate; for example, if you are using a sampling rate of 100 kSamples/s (100 kHz), specify a buffer size of 100,000 samples.

If any of these error conditions occurs, the board stops acquiring and transferring data to the host computer.

Note: DT-Open Layers reports any of these errors as an overrun message. In Windows NT 4.0, you can determine which of these errors generated the overrun message using the Event Viewer.

Analog Output Features

Two analog output (D / A) subsystems are provided on DT3010 Series boards. The first D / A subsystem contains the majority of analog output features. The second is dedicated to threshold triggering only (refer to page 45 for more information on analog threshold triggering).

This section describes the following features of the first D / A subsystem:

- Analog output resolution,
- Analog output channels,
- Output ranges and gains,
- Output filters,
- D / A output clock sources,
- Trigger sources,
- Analog output conversion modes,
- Data formats and transfer, and
- Error conditions.

Analog Output Resolution

DT3010, DT3010-268, DT3010 / 32, and DT3010 / 32-268 boards have a fixed analog output resolution of 12 bits. The DT3016 board has a fixed analog output resolution of 16 bits. The analog output resolution cannot be changed in software.

Analog Output Channels

DT3010 Series boards support two differential analog output channels (DAC0 and DAC1). Use software to specify the channel type. Refer to the *DT3010 Series Getting Started Manual* for information on how to wire analog output signals to the board using the screw terminal panel.

Within each DAC, the digital data is double buffered to prevent spurious outputs, then output as an analog signal. Both DACs power up to a value of 0 V ±10 mV. Note that resetting the board does not clear the values in the DACs.

DT3010 Series boards can output data from a single analog output channel or from two analog output channels. The following subsections describe how to specify the channels.

Specifying a Single Channel

The simplest way to output data to a single analog output channel is to specify the channel for a single-value analog output operation using software; refer to page 46 for more information on single-value operations.

You can also specify a single analog output channel using an analog output channel list, described in the next section.

Specifying One or More Channels

You can specify one or two analog output channels in the analog output channel list, either starting with DAC 0 or with DAC 1.

Values are output simultaneously to the entries in the channel list.

Output Filters

On the DT3016 board only, each DAC supports a software-selectable, single-pole, filter of 20 kHz. Specifying a 20 kHz filter is useful if you want to smooth the output values of the DAC.

On power-up or reset, no filter is used.

Output Ranges and Gains

Each DAC on the DT3010 Series board can output bipolar analog output signals in the range of ±10 V.

Through software, specify the range for the entire analog output subsystem as –10 V to +10 V, and the gain for each DAC as 1.

If you are using a single-value operation, specify a gain of 1; refer to page 46 for more information on single-value operations.

If you are using an analog output channel list, the subsystem defaults to a gain of 1 for each channel; therefore, you do not have to specify the gain.

D/A Output Clock Sources

DT3010 Series boards provide two clock sources for pacing the output of each channel in the analog output channel-gain list:

- An internal D/A output clock that uses the 24-bit D/A Counter on the board, and
- An external D/A output clock that you can connect to the screw terminal panel.

The following subsections describe the internal and external D/A output clocks in more detail.

Internal D/A Output Clock

The internal D/A output clock uses a 20 MHz time base. Conversions start on the falling edge of the counter output; the output pulse is active low.

Through software, specify the clock source as internal and the clock frequency at which to pace the analog output operation. The minimum frequency supported is 1.2 Hz (1.2 Samples/s). For DT3010, DT3010-268, DT3010/32, and DT3010/32-268 boards, the maximum frequency supported is 500 kHz (500 kSamples/s). For DT3016 boards, the maximum frequency supported is 200 kHz (200 kSamples/s). See page 46 for more information on these conversion modes.

External D/A Output Clock

The external D/A output clock is useful when you want to pace analog output operations at rates not available with the internal D/A output clock, if you want to pace at uneven intervals, or if you want to start pacing when an external event occurs.

Connect an external D/A output clock to screw terminal 74 on the DT740 screw terminal panel, screw terminal 46 on the STP268 screw terminal panel (attached to connector J1), or screw terminal 44 on the STP268-EC screw terminal panel. Conversions start on the falling edge of the external D/A output clock signal.

Using software, specify the clock source as external. For DT3010 Series boards, the clock frequency is always equal to the frequency of the external D/A output clock input signal that you connect to the board through the screw terminal panel.

Trigger Sources

A trigger is an event that occurs based on a specified set of conditions. DT3010 Series boards support the following trigger sources for analog output operations:

- Software trigger,
- External digital (TTL) trigger, and
- Analog threshold trigger.

This subsection describes these trigger sources in more detail.

Software Trigger

A software trigger event occurs when you start the analog output operation (the computer issues a write to the board to begin conversions). Specify the software trigger source in software.

External Digital (TTL) Trigger

For analog output operations, an external digital trigger event occurs when the DT3010 Series board detects either a rising or falling edge on the External D/A TTL Trigger input signal connected to screw terminal 75 on the DT740 screw terminal panel, screw terminal 45 on the STP268 screw terminal panel (attached to connector J1), or screw terminal 10 on the STP268-EC screw terminal panel. The trigger signal is TTL-compatible.

Using software, specify the trigger source as either a rising-edge external digital trigger (external for SDK users) or falling-edge external digital trigger (extra for SDK users)

Analog Threshold Trigger

For analog output operations, an analog trigger event occurs when the DT3010 Series board detects a transition from above a threshold level to below a threshold level (falling edge), or a transition from below a threshold level to above a threshold level (rising edge). The following analog threshold trigger sources are available:

- **External Analog Trigger input signal** connected to screw terminal 107 on the DT740 screw terminal panel, screw terminal 39 on the STP268 screw terminal panel (attached to connector J1), or screw terminal 15 on the STP268-EC screw terminal panel. Using software, specify the trigger source as either a rising-edge (extra+1 for DataAcq SDK users) or falling-edge analog threshold trigger (extra +2 for DataAcq SDK users).
- **One of the analog input channels** after gain is applied**.** Using software, specify the trigger source as either a positive threshold trigger or a negative threshold trigger.

  Using software, specify the analog input channel used as the analog threshold trigger as the first channel in the analog input channel list; refer to page 12 for more information.

  On DT3010 Series boards, the threshold level is set using a dedicated 8-bit DAC (the second analog output subsystem); the hysteresis is fixed at 50 mV. Using software, program the threshold level by writing a voltage value to the DAC of the second analog output subsystem; this value can range from –10 V to +10 V.

Note: If you are using an analog threshold trigger to trigger both the A / D and the D / A subsystems, ensure that you use the same analog trigger type for both subsystems (either external or one of the analog input channels). The polarity of the triggers, however, can be different.

Analog Output Conversion Modes

DT3010 Series boards support the following conversion modes:

- **Single-value operations** are the simplest to use but offer the least flexibility and efficiency. Use software to specify the range, gain, and analog output channel (among other parameters), and output the data from that channel. For a single-value operation, you cannot specify a clock source, trigger source, or buffer. Single-value operations stop automatically when finished; you cannot stop a single-value operation.

- **Continuous analog output operations** take full advantage of the capabilities of the DT3010 Series boards. In this mode, you can specify an analog input channel-gain list, clock source, trigger source, buffer, and buffer wrap mode. Two continuous analog output operations are supported: continuously-paced and waveform generation mode. These modes are described in the following subsections.

  To stop a continuously-paced analog output operation, you can stop sending data to the board, letting the board stop when it runs out of data, or you can perform either an orderly stop or an abrupt stop using software. In an orderly stop, the board finishes outputting the specified number of samples, then stops; all subsequent triggers are ignored. In an abrupt stop, the board stops outputting samples immediately; all subsequent triggers are ignored.

Continuously-Paced Analog Output

Use continuously-paced analog output mode if you want to accurately control the period between conversions of individual analog output channels in the analog output channel list.

The host computer transfers digital values to write to the DACs from allocated circular buffers in computer memory to the output FIFO on the board. DT3010, DT3010-268, and DT3016 boards have a 4 kSample output FIFO; DT3010/32 and DT3010/32-268 boards have a 32 kSample output FIFO for demanding analog output operations. Use software to allocate the number of buffers and to specify the values.

When it detects a trigger, the board outputs the values in the output FIFO to the DACs at the same time. Even samples (0, 2, 4, and so on) are written to entry 0 in the channel list; odd samples (1, 3, 5, and so on) are written to entry 1 in the channel list. The operation repeats continuously until either all the data is output from the buffers (if buffer wrap mode is none) or if you stop the operation (if buffer wrap mode is multiple). Refer to page 49 for more information on buffers.

Ensure that the host computer transfers data to the output FIFO fast enough so that the output FIFO does not empty completely; otherwise, an output FIFO underrun error results. Note that the output FIFO counter increments each time the host loads a value into the output FIFO and decrements each time the DAC reads a value from the output FIFO; the counter is reset to 0 when the output FIFO is reset. To avoid the output FIFO underrun error in continuously-paced mode, the host computer can read the output FIFO counter to determine how many samples remain in the output FIFO, and transfer more data before the output FIFO empties.

The conversion rate is determined by the frequency of the D/A output clock. For DT3010, DT3010-268, DT3010/32, and DT3010/32-268 boards, the maximum throughput rate in this mode is 500 kHz (500 kSamples/s) in 100 mV steps. For DT3016 boards, the maximum throughput rate in this mode is 200 kHz (200 kSamples/s) in 100 mV steps. Note that rate is system-dependent. Refer to page 42 for more information on the D/A output clock.

To select continuously-paced analog output mode, use software to specify the dataflow as continuous, the buffer wrap mode as multiple, and the trigger source as any of the supported trigger sources. Refer to page 44 for more information on the supported trigger sources.

Waveform Generation

Use waveform generation mode if you want to output waveforms repetitively.

Before this process can begin, the host computer must transfer the entire waveform pattern to output to the DACs from a single buffer allocated in computer memory into the output FIFO on the board. Use software to allocate the memory and the specify the waveform pattern.

For the DT3010, DT3010-268, and DT3016 boards, if you are using a single DAC, the waveform pattern can range from 2 to 4,096 samples; if you are using two DACs, the waveform pattern can range from 2 to 2,048 samples. For the DT3010/32 and DT3010/32-268 boards, if you are using a single DAC, the waveform pattern can range from 2 to 32,768 samples; if you are using two DACs, the waveform pattern can range from 2 to 16,384 samples. Specify both DACs in the analog output channel list.

When it detects a trigger, the board cycles through the analog output channel-gain list, converting and outputting the specified waveform for the specified DACs. When the output FIFO empties, the board issues a retransmit pulse to the output FIFO. This allows the board to output the same pattern continuously to the DACs without having to reload the output FIFOs. The buffer wrap mode must be single in this mode; refer to page 49 for more information on buffers.

The conversion rate is determined by the frequency of the D / A output clock. For DT3010, DT3010-268, DT3010 / 32, and DT3010 / 32-268 boards, the maximum throughput rate in this mode is 500 kHz (500 kSamples / s) in 100 mV steps. For the DT3016 boards, the maximum throughput rate in this mode is 200 kHz (200 kSamples / s) in 100 mV steps. Refer to page 42 for more information on the D / A output clock.

To select waveform generation mode, use software to specify the dataflow as continuous, the buffer wrap mode as single, and the trigger source as any of the supported trigger sources. Refer to page 44 for more information on the supported trigger sources.

Data Format and Transfer

Data from the host computer must use offset binary data encoding for analog output signals, such as 000 (for 12-bit boards) or 0000 (for 16-bit boards) to represent –10 V, and FFFh (for 12-bit boards) or FFFFh (for 16-bit boards) to represent +10 V. Using software, specify the data encoding as binary.

The host computer transfers data as 32-bit words from one or more allocated circular buffers in computer memory to the output FIFO on the board. DT3010 Series boards act as PCI slaves to the host computer when performing analog output operations.

The host computer must pack two output samples (an even and an odd sample) into each transfer to the DT3010 Series board. The even sample is written to the output FIFO first, followed by the odd sample. If the analog output channel list contains two DACs, the even samples (0, 2, 4, and so on) are written to channel entry 0 in the analog output channel-gain list; the odd samples (1, 3, 5, and so on) are written to channel entry 1 in the analog output channel-gain list. If the analog output channel list contains one DAC, all the samples are written to the DAC, alternating between even and odd samples.

Note that for continuously-paced analog output operations, the data from the circular buffers in host computer memory can wrap multiple times (wrap mode is multiple). That is, once all the data in the buffers is written to the output FIFO on the board, the process repeats continuously starting with the first location of the first buffer, until you stop it. If wrap mode is none, once all the data is output from the allocated buffers, the operation stops.

For waveform generation mode, the data from a single circular buffer is written once to the output FIFO on the board (wrap mode is single); the board then continuously outputs the data. That is, once all the data in the buffer is written to the output FIFO on the board, the host computer is finished transferring data; the board recycles the data in the output FIFO without using the bandwidth of the PCI bus or host processor, and the process repeats continuously until you stop the operation.

Error Conditions

DT3010 Series boards can report an output FIFO underflow error to the host computer. This error indicates that the analog output data was not being transferred fast enough across the PCI bus from the host computer to the output FIFO on the board.

If the D / A output clock occurs while the output FIFO is empty, an error is not reported since the most likely cause is that the host computer has no more data to output; in this case, the last value received from the host computer is output by the specified DACs continuously until the board is powered down or new data becomes available. If, however, the host does an additional write to the output FIFO (after the D / A output clock occurred while the output FIFO was empty), the data is written to the DACs and the output FIFO Underflow error is reported. This error has no effect on board operation; the host computer can clear this error.

To avoid this error, ensure that the host computer provides data to the output FIFO faster than the DACs are converting the data. You can read the value of the output FIFO counter to determine how many samples are in the output FIFO.

If this error condition occurs, the host computer stops transferring data to the board and the board continues to output the last data transferred to it by the host computer.

Digital I/O Features

This section describes the following features of the digital I/O subsystem:

- Digital I/O lines,
- Digital I/O resolution, and
- Digital I/O operation modes.

Digital I/O Lines

DT3010 Series boards support 16 digital I/O lines through the digital input (DIN) and output (DOUT) subsystems; both subsystems use the same digital I/O lines. These lines are divided into two banks of eight: Bank A, lines 0 to 7; and Bank B, lines 0 to 7. You can use each bank as either an input port or an output port; all eight lines within a bank have the same configuration. For example, if you use Bank A as an input port (port 0), lines 0 to 7 of Bank A are configured as inputs. Likewise, if you use Bank B as an output port (port 1), lines 0 to 7 of Bank B are configured as outputs.

Specify the digital I/O line to read or write in a single-value digital I/O operation; refer to page 53 for more information on single-value operations.

A digital line is high if its value is 1; a digital line is low if its value is 0.

On power up or reset, no digital data is output from the board.

Digital I/O Resolution

Using software, specify the number of banks to read by specifying the resolution as 8 (for eight lines) or 16 (for 16 lines). If you specify a resolution of 8, two digital I/O subsystems are available. Element 0 (the first subsystem) corresponds to the Bank A, lines 0 to 7. Element 1 (the second subsystem) corresponds to Bank B, lines 0 to 7. If you specify a resolution of 16, one subsystem is available.

Note: When the resolution is 16, digital I/O lines 0 to 7 of Bank B are represented as bits 8 to 15 of the digital value.

Digital I/O Operation Modes

DT3010 Series boards support the following digital I/O operation modes:

- **Single-value operations** are the simplest to use but offer the least flexibility and efficiency. Use software to specify the digital I/O line, and a gain of 1 (the gain is ignored). Data is then read from or written to the digital I/O line. For a single-value operation, you cannot specify a clock or trigger source.

  Single-value operations stop automatically when finished; you cannot stop a single-value operation.

- **Continuous digital input** takes full advantage of the capabilities of the DT3010 Series boards. In this mode, you enter all 16 digital input lines as channel 32 of the analog input channel-gain list using software. This mode is programmed through the A/D subsystem. Using this mode, you can specify a clock source, scan mode, trigger source, trigger acquisition mode, buffer, and buffer wrap mode for the digital input operation. Refer to page 13 for more information on specifying digital input lines for a continuous digital input operation.

- **Dynamic digital output** is useful for synchronizing and controlling external equipment and allows you to output data to two dynamic digital output lines each time an analog input value is acquired. This mode is programmed through the A/D subsystem; refer to page 14 for more information.

Counter/Timer Features

The counter / timer circuitry on the board provides the clocking circuitry used by the A / D and D / A subsystems as well as several user counter / timer features. This section describes the following user counter / timer features:

- Units,
- C / T clock sources,
- Gate types,
- Pulse types and duty cycles, and
- Counter / timer operation modes.

Units

DT3010 Series boards support four user 16-bit counter / timer units (called counters); counters are numbered 0, 1, 2, and 3.

Each counter accepts a clock input signal and gate input signal and outputs a clock output signal (also called a pulse output signal), as shown in Figure 9.

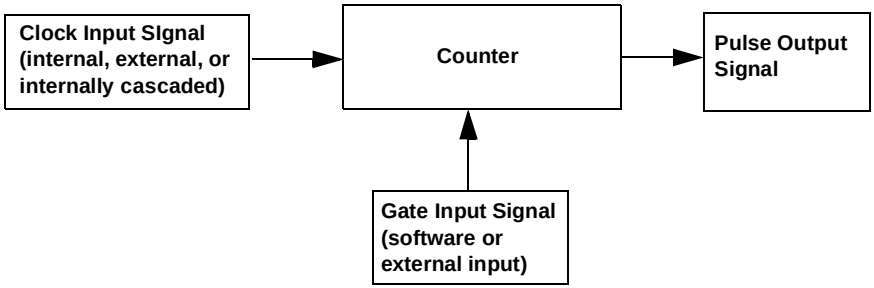

Clock Input SIgnal (internal, external, or internally cascaded)
Counter
Pulse Output Signal
Gate Input Signal (software or external input)

Figure 9: Counter/Timer Channel

Each counter corresponds to a counter/timer (C/T) subsystem. To specify the counter to use in software, specify the appropriate C/T subsystem. For example, counter 0 corresponds to C/T subsystem element 0; counter 3 corresponds to C/T subsystem element 3.

C/T Clock Sources

The following clock sources are available for the user counters:

- Internal C/T clock,
- External C/T clock, and
- Internally cascaded clock.

Refer to the following subsections for more information on these clock sources.

Internal C/T Clock

The internal C/T clock uses a 20 MHz time base. Counter/timer operations start on the rising edge of the clock input signal.

Through software, specify the clock source as internal and the frequency at which to pace the counter/timer operation (this is the frequency of the clock output signal). The maximum frequency that you can specify for the clock output signal is 10 MHz. The minimum frequency that you can specify for the clock output signal is 305.18 Hz.

External C/T Clock

The external C/T clock is useful when you want to pace counter/timer operations at rates not available with the internal C/T clock or if you want to pace at uneven intervals. The rising edge of the external C/T clock input signal is the active edge.

Using software, specify the clock source as external and the clock divider used to determine the frequency at which to pace the operation (this is the frequency of the clock output signal). The minimum clock divider that you can specify is 2.0; the maximum clock divider that you can specify is 65,536. For example, if you supply an external C/T clock with a frequency of 5 MHz and specify a clock divider of 5, the resulting frequency of the external C/T clock output signal is 1 MHz. The resulting frequency of the external C/T clock output signal must not exceed 2.5 MHz.

Connect the external C/T clock to the board through the DT740, STP268, or STP268-EC screw terminal panel. Table 3 lists the screw terminals that correspond to the external C/T clock signals of each counter/timer.

Table 3: External C/T Clock Input Signals

Counter/Timer	Screw Terminal on the DT740	Screw Terminal on the STP268	Screw Terminal on the STP268-EC
0	TB58	TB54 (STP268 must be attached to connector J1)	TB5
1	TB62	TB58 (STP268 must be attached to connector J1)	TB38
2	TB66	TB54 (STP268 must be attached to connector J2)	– α
3	TB70	TB58 (STP268 must be attached to connector J2)	–[a]

a. To access counter/timers 2 or 3, connect an STP268 screw terminal panel to connector J2 on the DT3010-268 board.

Internally Cascaded Clock

You can also internally route the clock output signal from one user counter to the clock input signal of the next user counter to internally cascade the counters. In this way, you can create a 32-bit counter without externally connecting two counters together. DT3010 Series boards support software cascading on counters 0 and 1, 1 and 2, and 2 and 3.

Specify internal cascade mode in software. The rising edge of the clock input signal is active.

Through software, specify the clock source as internal and the frequency at which to pace the counter/timer operation (this is the frequency of the clock output signal). The maximum frequency that you can specify for the clock output signal is 10 MHz. For a 32-bit cascaded counter, the minimum frequency that you can specify for the clock output signal is 0.00465 Hz, which corresponds to a rate of once every 215 seconds.

Note: In software, specify the clock input and gate input for the first counter in the cascaded pair. For example, if counters 1 and 2 are cascaded, specify the clock input and gate input for counter 1.

Gate Types

The active edge or level of the gate input to the counter enables counter / timer operations. The operation starts when the clock input signal is received. DT3010 Series boards provide the following gate input types:

- **None** – A software command enables any specified counter / timer operation immediately after execution. This gate type is useful for all counter / timer modes.
- **Logic-low level external gate input** – Enables a counter / timer operation when the external gate signal is low, and disables the counter / timer operation when the external gate signal is high. Note that this gate type is used only for event counting, frequency measurement, and rate generation; refer to page 62 for more information on these modes.
- **Logic-high level external gate input** – Enables a counter / timer operation when the external gate signal is high, and disables a counter / timer operation when the external gate signal is low. Note that this gate type is used only for event counting, frequency measurement, and rate generation; refer to page 62 for more information on these modes.
- **Falling-edge external gate input** – Enables a counter / timer operation on the transition from the high level to the low level (falling edge). In software, this is called a low-edge gate type. Note that this gate type is used only for one-shot and repetitive one-shot mode; refer to page 75 for more information on these modes.
- **Rising-edge external gate input** – Enables a counter / timer operation on the transition from the low level to the high level (rising edge). In software, this is called a high-edge gate type. Note that this gate type is used only for one-shot and repetitive one-shot mode; refer to page 75 for more information on these modes.

Specify that gate type in software.

Table 4 lists the screw terminals that correspond to the gate input signals of each counter / timer.

Table 4: Gate Input Signals

Counter/Timer	Screw Terminal on the DT740	Screw Terminal on the STP268	Screw Terminal on the STP268-EC
0	TB60	TB56 (STP268 must be attached to connector J1)	TB37
1	TB64	TB60 (STP268 must be attached to connector J1)	TB36
2	TB68	TB56 (STP268 must be attached to connector J2)	– α
3	TB72	TB60 (STP268 must be attached to connector J2)	–[a]

a. To access counter / timers 2 or 3, connect an STP268 screw terminal panel to connector J2 on the DT3010-268 board.

Pulse Output Types and Duty Cycles

The DT3010 Series boards can output pulses from each counter / timer. Table 5 lists the screw terminals that correspond to the pulse output signals of each counter / timer.

Table 5: Pulse Output Signals

Counter/Timer	Screw Terminal on the DT740	Screw Terminal on the STP268	Screw Terminal on the STP268-EC
0	TB59	TB55 (STP268 must be attached to connector J1)	TB3
1	TB63	TB59 (STP268 must be attached to connector J1)	TB2
2	TB67	TB55 (STP268 must be attached to connector J2)	– [a]
3	TB71	TB59 (STP268 must be attached to connector J2)	–[a]

a. To access counter/timers 2 or 3, connect an STP268 screw terminal panel to connector J2 on the DT3010-268 board.

DT3010 Series boards support the following pulse output types on the clock output signal:

- **High-to-low transitions** - The low portion of the total pulse output period is the active portion of the counter/timer clock output signal.
- **Low-to-high transitions** - The high portion of the total pulse output period is the active portion of the counter/timer pulse output signal.

You specify the pulse output type in software.

The duty cycle (or pulse width) indicates the percentage of the total pulse output period that is active. A duty cycle of 50, then, indicates that half of the total pulse is low and half of the total pulse output is high. You specify the duty cycle in software.

Figure 10 illustrates a low-to-high pulse with a duty cycle of approximately 30%.

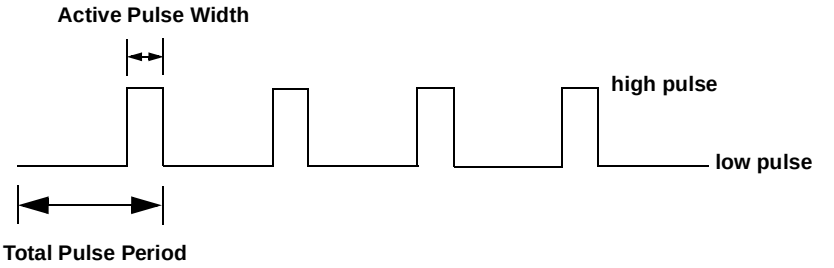


Figure 10: Example of a Low-to-High Pulse Output Type

Counter/Timer Operation Modes

DT3010 Series boards support the following counter / timer operation modes:

- Event counting,
- Frequency measurement,
- Rate generation,
- One-shot, and
- Repetitive one-shot.

The following subsections describe these modes in more detail.

Event Counting

Use event counting mode to count events from the counter's associated clock input source.

If you are using one counter, you can count a maximum of 65,536 events before the counter rolls over to 0 and starts counting again. If you are using a cascaded 32-bit counter, you can count a maximum of 4,294,967,296 events before the counter rolls over to 0 and starts counting again.

In event counting mode, use an external C/T clock source; refer to page 56 for more information on the external C/T clock source.

Using software, specify the counter/timer mode as event counting (count), the C/T clock source as external, and the gate type that enables the operation. Refer to page 60 for information on gates.

Ensure that the signals are wired appropriately. Figure 11 shows one example of connecting an event counting application. This example uses the DT740 screw terminal panel and user counter 0; rising clock edges are counted while the gate is active.

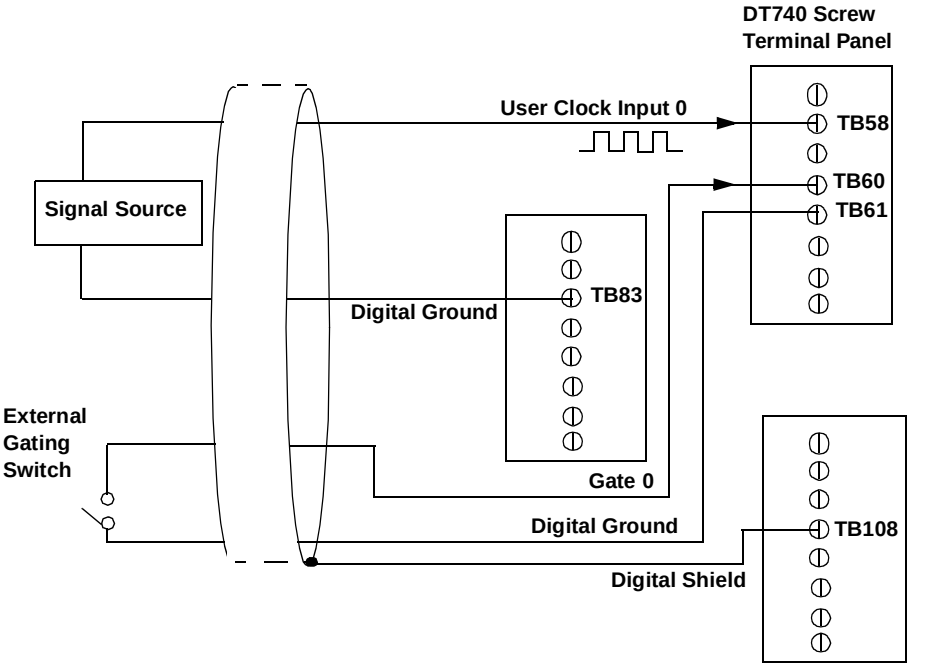


Figure 11: Connecting Event Counting Signals (Shown for Clock Input 0 and External Gate 0)

Figure 12 shows an example of an event counting operation. In this example, the gate type is low level.

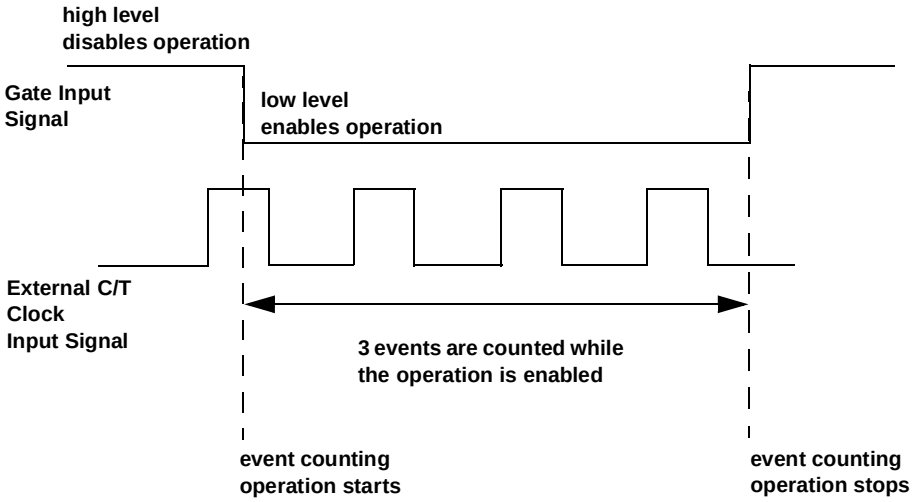


Figure 12: Example of Event Counting

Frequency Measurement

Use frequency measurement mode to measure the frequency of the signal from counter's associated clock input source over a specified duration. In this mode, use an external C/T clock source; refer to page 56 for more information on the external C/T clock source.

One way to perform a frequency measurement is to use the same wiring as an event counting application that does not use an external gate signal, as shown in Figure 13.

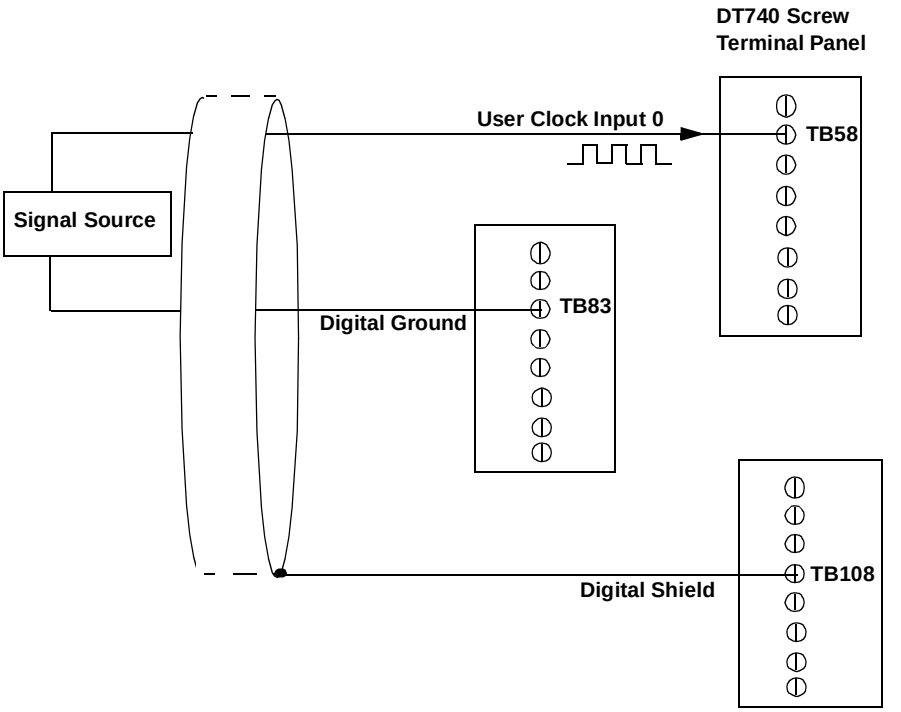


Figure 13: Connecting Frequency Measurement Signals without an External Gate Input (Shown for Clock Input 0)

In this configuration, use software to specify the counter/timer mode as frequency measurement or event counting, and the duration of the Windows timer over which to measure the frequency. (The Windows timer uses a resolution of 1 ms.) In this configuration, frequency is determined using the following equation:

$$\text{Frequency Measurement} = \frac{\text{Number of Events}}{\text{Duration of the Windows Timer}}$$

If you need more accuracy than the Windows timer provides, you can connect a pulse of a known duration (such as a one-shot output of another user counter) to the external gate input, as shown in Figure 14.

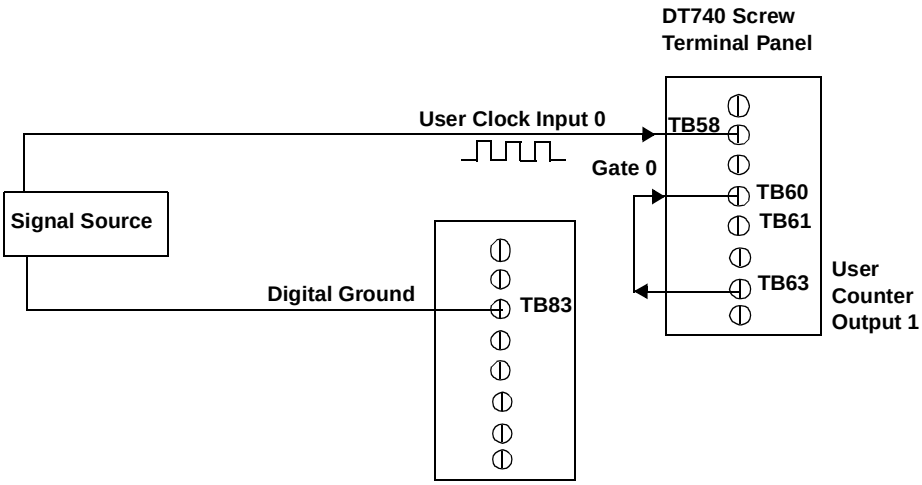


Figure 14: Connecting Frequency Measurement Signals (Shown for Clock Input 0 and External Gate 0)

In this configuration, use software to set up the counter/timers as follows:

1. Set up one of the counter/timers for one-shot mode, specifying the clock source, clock frequency, gate type, type of output pulse (high or low), and pulse width.
2. Set up the counter/timer that will measure the frequency for event counting mode, specifying the clock source to count, and the gate type (this should match the pulse output type of the counter/timer set up for one-shot mode).

3. Start both counters (events are not counted until the active period of the one-shot pulse is generated).
4. Read the number of events counted. (Allow enough time to ensure that the active period of the one-shot occurred and that events have been counted.)
5. Determine the measurement period using the following equation:

$$\text{Measurement period} = \frac{1}{\text{Clock Frequency}} * \text{Active Pulse Width}$$

6. Determine the frequency of the clock input signal using the following equation:

$$\text{Frequency Measurement} = \frac{\text{Number of Events}}{\text{Measurement Period}}$$

Figure 15 shows an example of a frequency measurement operation. In this example, three events are counted during a duration of 300 ms. The frequency, then, is 10 Hz, since 10 Hz = 3/(.3 s).

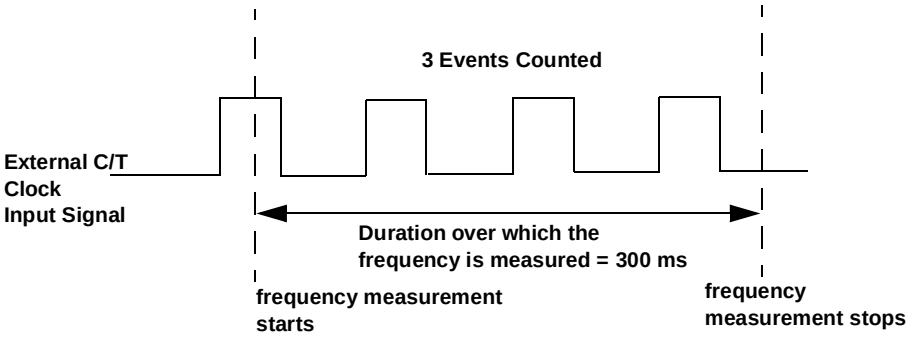


Figure 15: Example of Frequency Measurement

Rate Generation

Use rate generation mode to generate a continuous pulse output signal from the counter; this mode is sometimes referred to as continuous pulse output or pulse train output. You can use this pulse output signal as an external clock to pace other operations, such as analog input, analog output, or other counter/timer operations.

While the pulse output operation is enabled, the counter outputs a pulse of the specified type and frequency continuously. As soon as the operation is disabled, rate generation stops.

The period of the output pulse is determined by the clock input signal and the external clock divider. If you are using one counter (not cascaded), you can output pulses using a maximum frequency of 10 MHz (this is the frequency of the clock output signal). In rate generation mode, either the internal or external C/T clock input source is appropriate depending on your application; refer to page 56 for more information on the C/T clock source.

Using software, specify the counter/timer mode as rate generation (rate), the C/T clock source as either internal or external, the polarity of the output pulses (high-to-low transitions or low-to-high transitions), the duty cycle of the output pulses, and the gate type that enables the operation. Refer to page 60 for more information on pulse output signals and to page 59 for more information on gate types.

Ensure that the signals are wired appropriately. Figure 16 shows one example of connecting a pulse output operation. This example uses the DT740 screw terminal panel, user counter 0, and a software gate type.

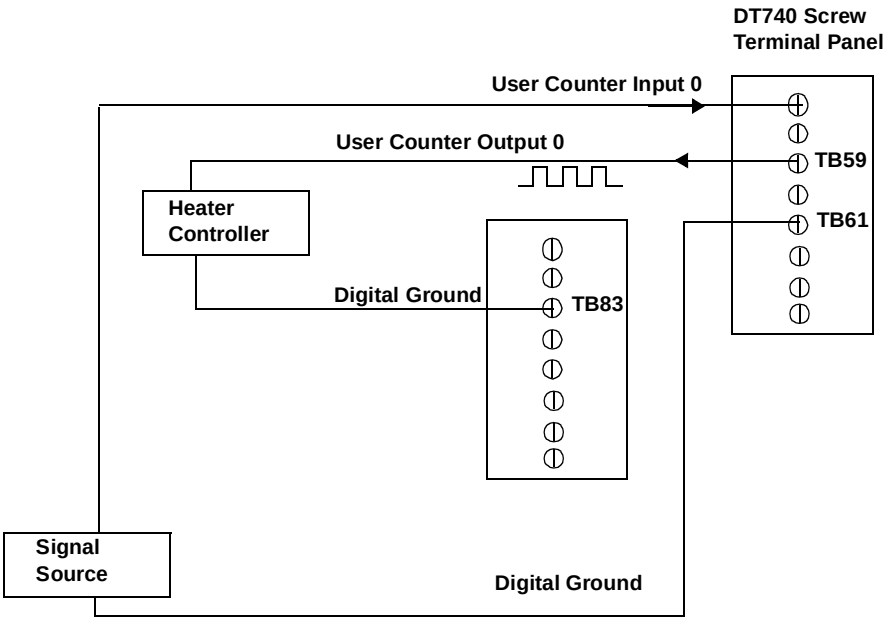


Figure 16: Connecting Rate Generation Signals (Shown for Counter Output 0; a Software Gate is Used)

Figure 17 shows an example of an enabled rate generation operation using an external C/T clock source with an input frequency of 4 kHz, a clock divider of 4, a low-to-high pulse type, and a duty cycle of 75%. (The gate type does not matter for this example.) A 1 kHz square wave is the generated output. Figure 18 shows the same example using a duty cycle of 25%.

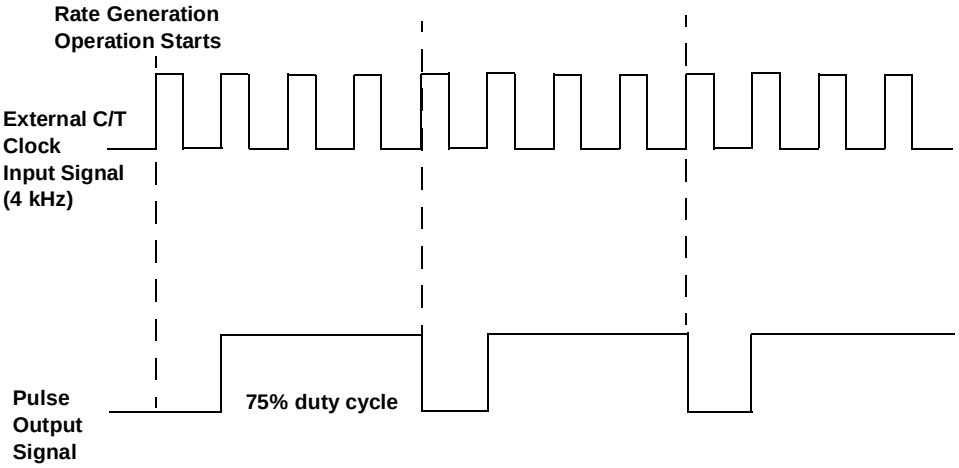


Figure 17: Example of Rate Generation Mode with a 75% Duty Cycle

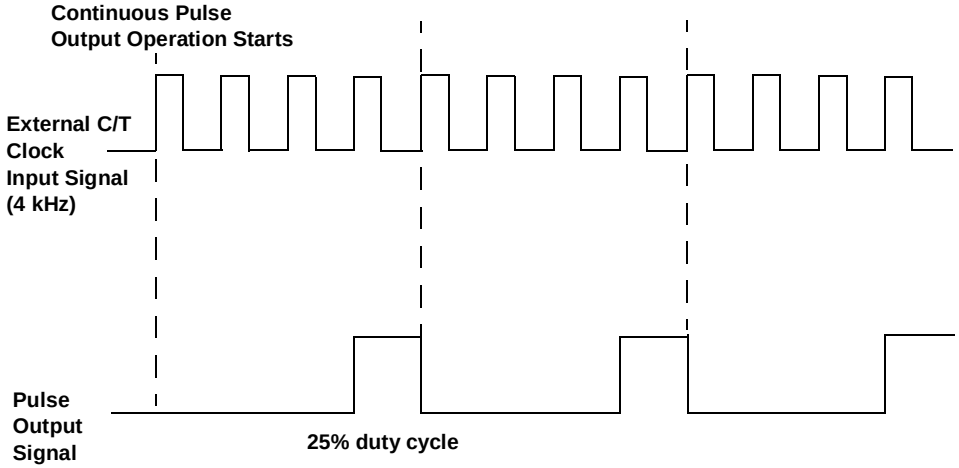


Figure 18: Example of Rate Generation Mode with a 25% Duty Cycle

One-Shot

Use one-shot mode to generate a single pulse output signal from the counter when the operation is triggered (determined by the gate input signal). You can use this pulse output signal as an external digital (TTL) trigger to start other operations, such as analog input or analog output operations.

When the one-shot operation is triggered, a single pulse is output; then, the one-shot operation stops. All subsequent clock input signals and gate input signals are ignored.

The period of the output pulse is determined by the clock input signal. In one-shot mode, the internal C/T clock source is more useful than an external C/T clock source; refer to page 56 for more information on the internal C/T clock source.

Using software, specify the counter/timer mode as one-shot, the clock source as internal, the polarity of the output pulse (high-to-low transition or low-to-high transition), the duty cycle of the output pulse, and the gate type to trigger the operation. Refer to page 60 for more information on pulse output types and to page 59 for more information on gate types.

Note: In the case of a one-shot operation, use a duty cycle as close to 100% as possible to output a pulse immediately. Using a duty cycle closer to 0% acts as a pulse output delay.

Ensure that the signals are wired appropriately. Figure 19 shows one example of connecting a pulse output operation. This example uses the DT740 screw terminal panel and user counter 0.

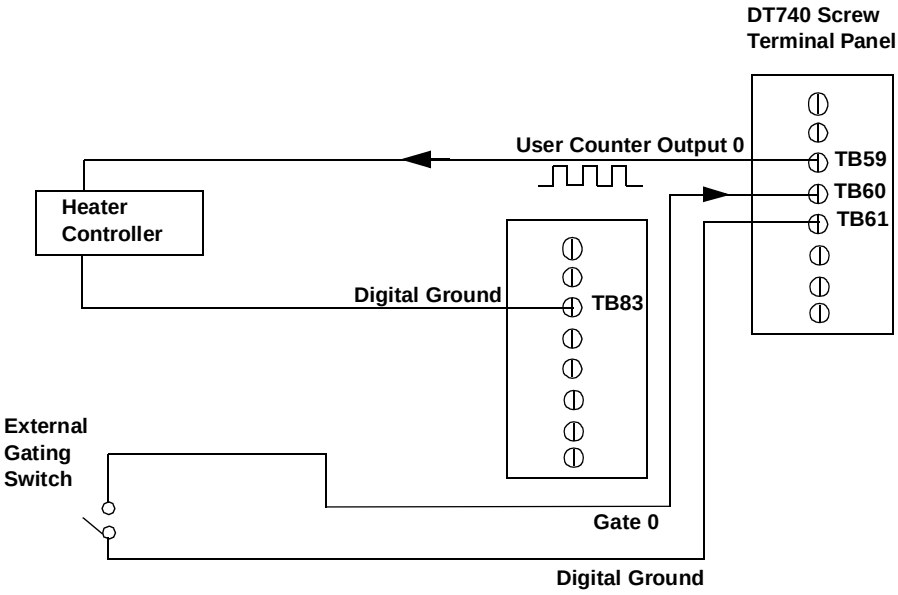


Figure 19: Connecting One-Shot Signals
(Shown for Counter Output 0 and Gate 0)

Figure 20 shows an example of a one-shot operation using an external gate input (rising edge), a clock output frequency of 1 kHz (pulse period of 1 ms), a low-to-high pulse type, and a duty cycle of 99.99%. Figure 21 shows the same example using a duty cycle of 50%.

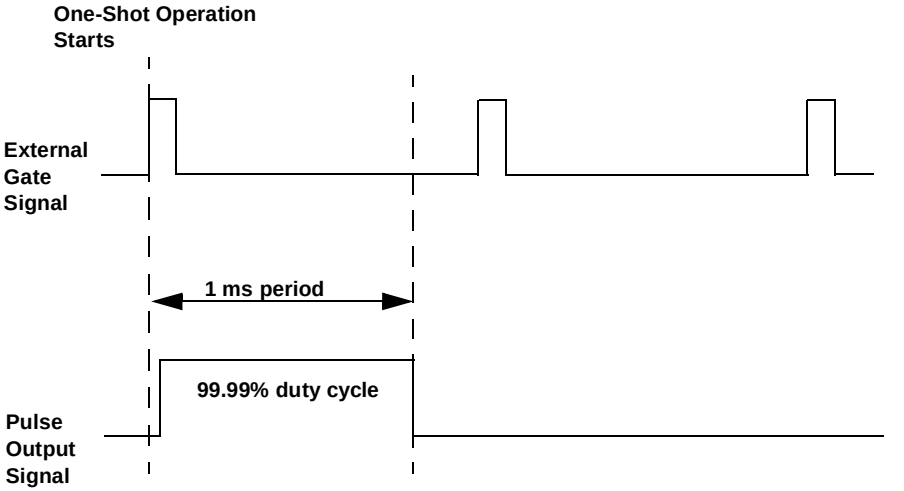


Figure 20: Example of One-Shot Mode Using a 99.99% Duty Cycle

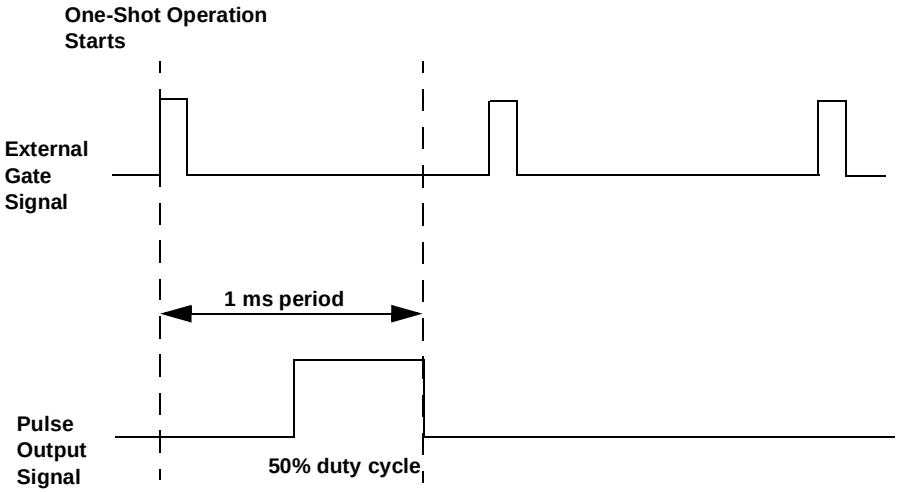


Figure 21: Example of One-Shot Mode Using a 50% Duty Cycle

Repetitive One-Shot

Use repetitive one-shot mode to generate a pulse output signal each time the board detects a trigger (determined by the gate input signal). You can use this mode to clean up a poor clock input signal by changing its pulse width, then outputting it.

In repetitive one-shot mode, the internal C/T clock source is more useful than an external C/T clock source; refer to page 56 for more information on the internal C/T clock source.

Use software to specify the counter/timer mode as repetitive one-shot (oneshot-rpt for SDK users), the polarity of the output pulses (high-to-low transitions or low-to-high transitions), the duty cycle of the output pulses, the C/T clock source, and the gate type to trigger the operation. Refer to page 60 for more information on pulse output types and to page 59 for more information on gates.

Note: In the case of a one-shot operation, use a duty cycle as close to 100% as possible to output a pulse immediately. Using a duty cycle closer to 0% acts as a pulse output delay.

When the one-shot operation is triggered (determined by the gate input signal), a pulse is output. When the board detects the next trigger, another pulse is output. This operation continues until you stop the operation.

Note: Triggers that occur while the pulse is being output are not detected by the board.

Figure 22 shows an example of a repetitive one-shot operation using the DT740 screw terminal panel, an external gate (rising edge), a clock output frequency of 1 kHz (one pulse every 1 ms), a low-to-high pulse type, and a duty cycle of 99.99%. Figure 23 shows the same example using a duty cycle of 50%.

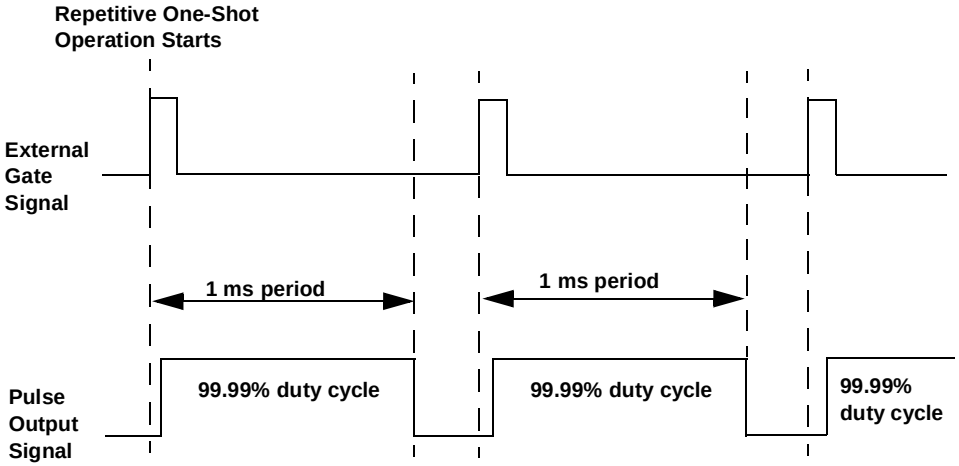


Figure 22: Example of Repetitive One-Shot Mode Using a 99.99% Duty Cycle

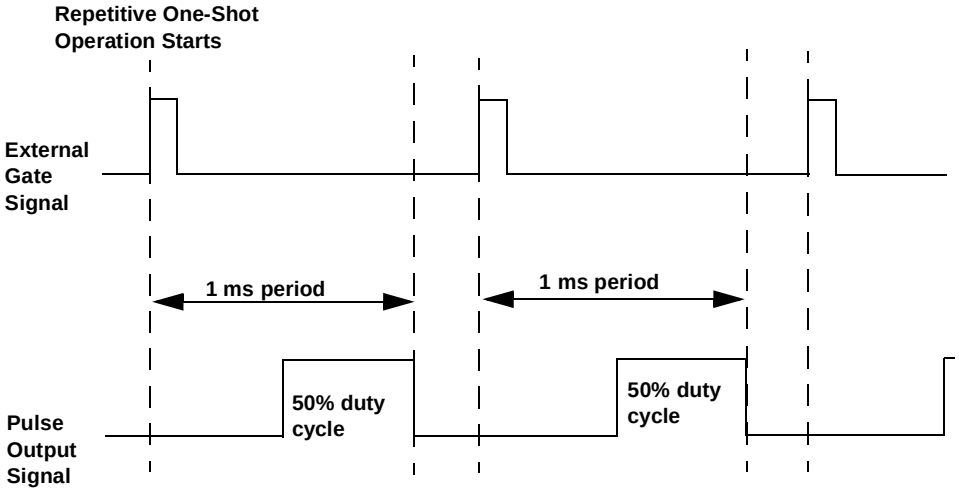


Figure 23: Example of Repetitive One-Shot Mode Using a 50% Duty Cycle

Synchronizing A/D and D/A Subsystems

You can synchronize the operation of the A / D and D / A subsystems providing that they are not performing single-value operations. Refer to page 20 and page 46 for more information on single-value operations.

You can synchronize the A / D and D / A subsystems in two ways: by synchronizing the triggers and by synchronizing the clocks. This section describes these two methods.

Synchronizing the Triggers

You can synchronize the triggers of the A / D and D / A subsystems as follows:

- **Software trigger** – Using software, specify the trigger source for the A / D and D / A subsystems as the software trigger. Then, using software, allocate a start list, put the A / D and D / A subsystems on the start list, prestart the subsystems, and start the subsystems. When started, both subsystems are triggered simultaneously.
- **External digital (TTL) trigger** – Using software, specify the trigger source for the A / D and D / A subsystems as the external digital (TTL) trigger. Then, wire an external digital TTL trigger to both the A / D subsystem and the D / A subsystem. Using software, allocate a start list, put the A / D and D / A subsystems on the start list, prestart the subsystems, then start the subsystems. When started, both subsystems are triggered simultaneously when the external digital event occurs.

- **External Analog threshold trigger** – Using software, specify the trigger source for the A/D and D/A subsystems as the external analog threshold trigger. Then, wire an external analog threshold trigger to the screw terminal panel. Using software, allocate a start list, put the A/D and D/A subsystems on the start list, prestart the subsystems, then start the subsystems. When started, both subsystems are triggered simultaneously when the external analog event occurs.
- **One of the analog input channels** – Using software, specify the trigger source for the A/D and D/A subsystems as one of the analog input channels. Then, wire an external analog threshold trigger to one of the 32 or 16 analog input channels (depending on the channel type specified). Using software, allocate a start list, put the A/D and D/A subsystems on the start list, prestart the subsystems, then start the subsystems. When started, both subsystems are triggered simultaneously when the external analog event occurs on the specified analog input channel.

Synchronizing the Clocks

You can synchronize the clocks of the A/D and D/A subsystems as follows:

- **Internal Sample Clocks** – Using software, specify the clock source as the internal A/D sample clock for the A/D subsystem and the internal D/A output clock for the D/A subsystem. Specify the same frequency for both internal clock sources. Then, specify the trigger source for the A/D and D/A subsystems as the software trigger. When started, both subsystems are triggered and clocked simultaneously.

- **External Sample Clocks** – Using software, specify the clock source as the external A / D sample clock for the A / D subsystem and as the external D / A output clock for the D / A subsystem. Then, wire an external sample clock to both the A / D subsystem and the D / A subsystem. Then, specify a synchronous trigger source for the A / D and D / A subsystems (refer to page 78). When started, both subsystems are triggered and clocked simultaneously.

3

Supported Capabilities

The DT3010 Series Device Driver provides support for analog input (A/D), analog output (D/A), digital input (DIN), digital output (DOUT), and counter/timer (C/T) subsystems. For information on how to install the device driver, refer to the *DT3010 Series Getting Started Manual*.

Table 6 summarizes the DT3010 Series capabilities available for use with the DataAcq SDK. The DataAcq SDK provides functions that return support information for specified subsystem capabilities at runtime.

The first row in the table lists the subsystem types. The first column in the table lists all possible subsystem capabilities. A description of each capability is followed by the parameter used to describe that capability in the DataAcq SDK.

Note: Blank fields represent unsupported options.

The DataAcq SDK uses the functions **olDaGetSSCaps** (for those queries starting with OLSSC) and **olDaGetSSCapsEx** (for those queries starting with OLSSCE) to return the supported subsystem capabilities for a device.

For more information, refer to the description of these functions in the DataAcq SDK online help. See the *DataAcq User's Manual* (UM-18326) for information on launching this help file.

Table 6: DT3010 Series Supported Option s

	DT3010 Series	A/D	D/A	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2[a]**	**2[b]**	**2[b]**	**0**	**4**
Data Flow Mode	Single-Value Operation Support OLSSC_SUP_SINGLEVALUE	Yes	Yes	Yes	Yes		
	Continuous Operation Support OLSSC_SUP_CONTINUOUS	Yes	Yes	No[c]			Yes
	Continuous Operation until Trigger Event Support OLSSC_SUP_CONTINUOUS_PRETRIG	Yes					
	Continuous Operation before and after Trigger Event OLSSC_SUP_CONTINUOUS_ABOUTTRIG	Yes					
	DT-Connect Support OLSSC_SUP_DTCONNECT						
	Continuous DT-Connect Support OLSSC_SUP_DTCONNECT_CONTINUOUS						
	Burst DT-Connect Support OLSSC_SUP_DTCONNECT_BURST						
Sim. Oper.	Simultaneous Start List Support OLSSC_SUP_SIMULTANEOUS_START	Yes	Yes				
Pause Oper.	Pause Operation Support OLSSC_SUP_PAUSE						
Wind. Mess.	Asynchronous Operation Support OLSSC_SUP_POSTMESSAGE	Yes	Yes				Yes
Buffering	Buffer Support OLSSC_SUP_BUFFERING	Yes	Yes				
	Single Buffer Wrap Mode Support OLSSC_SUP_WRPSINGLE	Yes	Yes				

Table 6: DT3010 Series Supported Options (cont.)

	DT3010 Series	A/D	D/A	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2[a]**	**2[b]**	**2[b]**	**0**	**4**
Buffering (cont.)	Multiple Buffer Wrap Mode Support OLSSC_SUP_WRPMULTIPLE	Yes	Yes				
	Inprocess Buffer Flush Support OLSSC_SUP_INPROCESSFLUSH	Yes					
DMA	Number of DMA Channels OLSSC_NUMDMACHANS	0	0	0	0		0
	Supports Gap Free Data with No DMA OLSSC_SUP_GAPFREE_NODMA	Yes	Yes				
	Supports Gap Free Data with Single DMA OLSSC_SUP_GAPFREE_SINGLEDMA						
	Supports Gap Free Data with Dual DMA OLSSC_SUP_GAPFREE_DUALDMA						
Triggered Scan Mode	Triggered Scan Support OLSSC_SUP_TRIGSCAN	Yes					
	Maximum Number of CGL Scans per Trigger OLSSC_MAXMULTISCAN	256[d]	0	0	0		0
	Supports Scan per Trigger Event Triggered Scan OLSSC_SUP_RETRIGGER_SCAN_PER_TRIGGER	Yes					
	Supports Internal Retriggered Triggered Scan OLSSC_SUP_RETRIGGER_INTERNAL	Yes					
	Extra Retrigger Support OLSSC_SUP_RETRIGGER_EXTRA	Yes					

Table 6: DT3010 Series Supported Options (cont.)

	DT3010 Series	A/D	D/A	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2[a]**	**2[b]**	**2[b]**	**0**	**4**
Triggered Scan Mode (cont.)	Maximum Retrigger Frequency OLSSCE_MAXRETRIGGER	357.14 kHz or 166.67 kHz[e]	0	0	0		0
	Minimum Retrigger Frequency OLSSCE_MINRETRIGGER	1.2 Hz[f]	0	0	0		0
Channel-Gain List	Maximum Channel-Gain List Depth OLSSC_CGLDEPTH	1024	2	1[c]	1[c]		0
	Sequential Channel-Gain List Support OLSSC_SUP_SEQUENTIAL_CGL	Yes	Yes				
	Zero Start Sequential Channel-Gain List Support OLSSC_SUP_ZEROSEQUENTIAL_CGL	Yes	Yes				
	Random Channel-Gain List Support OLSSC_SUP_RANDOM_CGL	Yes	Yes				
	Simultaneous Sample-and-Hold Support OLSSC_SUP_SIMULTANEOUS_SH						
	Channel List Inhibit Support OLSSC_SUP_CHANNELLIST_INHIBIT	Yes					
Gain	Programmable Gain Support OLSSC_SUP_PROGRAMGAIN	Yes					
	Number of Gains OLSSC_NUMGAINS	4	1	1	1		0
	AutoRanging Support OLSSC_SINGLEVALUE_AUTORANGE						

Table 6: DT3010 Series Supported Options (cont.)

	DT3010 Series	A/D	D/A	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2[a]**	**2[b]**	**2[b]**	**0**	**4**
Synchronous Digital I/O	Synchronous Digital I/O Support OLSSC_SUP_SYNCHRONOUS_DIGITALIO	Yes					
	Maximum Synchronous Digital I/O Value OLSSC_MAX_DIGITALIOLIST_VALUE	3	0	0	0		0
I/O Channels	Number of Channels OLSSC_NUMCHANNELS	33[g]	2	1	1		0
	DT2896 Channel Expansion Support OLSSC_SUP_EXP2896						
	DT727 Channel Expansion OLSSC_SUP_EXP727						
Channel Type	SE Support OLSSC_SUP_SINGLEENDED	Yes					
	SE Channels OLSSC_MAXSECHANS	32	0	0	0		0
	DI Support OLSSC_SUP_DIFFERENTIAL	Yes	Yes	Yes	Yes		
	DI Channels OLSSC_MAXDICHANS	16	2	1	1		0
Filters	Filter/Channel Support OLSSC_SUP_FILTERPERCHAN		Yes[h]				
	Number of Filters OLSSC_NUMFILTERS	1	2[h]	1	1		0
Ranges	Number of Voltage Ranges OLSSC_NUMRANGES	2	1	0	0		0
	Range per Channel Support OLSSC_SUP_RANGEPERCHANNEL						

Table 6: DT3010 Series Supported Options (cont.)

	DT3010 Series	A/D	D/A	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2[a]**	**2[b]**	**2[b]**	**0**	**4**
Resolution	Software Programmable Resolution OLSSC_SUP_SWRESOLUTION			Yes	Yes		
	Number of Resolutions OLSSC_NUMRESOLUTIONS	1[i]	1[i]	2[j]	2[j]		1
Data Encoding	Binary Encoding Support OLSSC_SUP_BINARY	Yes	Yes	Yes	Yes		Yes
	Twos Complement Support OLSSC_SUP_2SCOMP						
Triggers	Software Trigger Support OLSSC_SUP_SOFTTRIG	Yes	Yes				Yes
	External Trigger Support OLSSC_SUP_EXTERNTRIG	Yes[k]	Yes[k]				Yes
	Positive Threshold Trigger Support OLSSC_SUP_THRESHTRIGPOS	Yes[k]	Yes[k]				
	Negative Threshold Trigger Support OLSSC_SUP_THRESHTRIGNEG	Yes[k]	Yes[k]				
	Analog Event Trigger Support OLSSC_SUP_ANALOGEVENTTRIG						
	Digital Event Trigger Support OLSSC_SUP_DIGITALEVENTTRIG						
	Timer Event Trigger Support OLSSC_SUP_TIMEREVENTTRIG						
	Number of Extra Triggers OLSSC_NUMEXTRATRIGGERS	3[k]	3[k]	0	0		0

Table 6: DT3010 Series Supported Options (cont.)

	DT3010 Series	A/D	D/A	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2[a]**	**2[b]**	**2[b]**	**0**	**4**
Clocks	Internal Clock Support OLSSC_SUP_INTCLOCK	Yes	Yes				Yes
	External Clock Support OLSSC_SUP_EXTCLOCK	Yes	Yes				Yes
	Number of Extra Clocks OLSSC_NUMEXTRACLOCKS	0	0	0	0		0
	Base Clock Frequency OLSSCE_BASECLOCK	20 MHz	20 MHz	0	0		20 MHz
	Maximum External Clock Divider OLSSCE_MAXCLOCKDIVIDER	1.0	1.0	1.0	1.0		65536
	Minimum External Clock Divider OLSSCE_MINCLOCKDIVIDER	1.0	1.0	1.0	1.0		2.0
	Maximum Throughput OLSSCE_MAX_THROUGHPUT	1.25 MHz or 250 kHz[l]	500 kHz or 200 kHz[m]	0	0		10 MHz[n]
	Minimum Throughput OLSSCE_MIN_THROUGHPUT	1.2 Hz	1.2 Hz	0	0		0.005 Hz[o]
Counter/Timers	Cascading Support OLSSC_SUP_CASCADING						Yes
	Event Count Mode Support OLSC_SUP_CTMODE_COUNT						Yes
	Generate Rate Mode Support OLSSC_SUP_CTMODE_RATE						Yes
	One-Shot Mode Support OLSSC_SUP_CTMODE_ONESHOT						Yes
	Repetitive One-Shot Mode Support OLSSC_SUP_CTMODE_ONESHOT_RPT						Yes

Table 6: DT3010 Series Supported Options (cont.)

	DT3010 Series	A/D	D/A	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2[a]**	**2[b]**	**2[b]**	**0**	**4**
Counter/Timers (cont.)	High to Low Output Pulse Support OLSSC_SUP_PLS_HIGH2LOW						Yes
	Low to High Output Pulse Support OLSSC_SUP_PLS_LOW2HIGH						Yes
	None (internal) Gate Type Support OLSSC_SUP_GATE_NONE						Yes
	High Level GateType Support OLSSC_SUP_GATE_HIGH_LEVEL						Yes[p]
	Low Level Gate Type Support OLSSC_SUP_GATE_LOW_LEVEL						Yes[p]
	High Edge Gate Type Support OLSSC_SUP_GATE_HIGH_EDGE						Yes[p]
	Low Edge Gate Type Support OLSSC_SUP_GATE_LOW_EDGE						Yes[p]
	Level Change Gate Type Support OLSSC_SUP_GATE_LEVEL						
	High Level GateType with Input Debounce Support OLSSC_SUP_GATE_HIGH_LEVEL_DEBOUNCE						
	Low Level Gate Type with Input Debounce Support OLSSC_SUP_GATE_LOW_LEVEL_DEBOUNCE						
	High Edge Gate Type with Input Debounce Support OLSSC_SUP_GATE_HIGH_EDGE_DEBOUNCE						

Table 6: DT3010 Series Supported Options (cont.)

	DT3010 Series	A/D	D/A	DIN	DOUT	SRL	C/T
	Total Subsystems on Board	**1**	**2[a]**	**2[b]**	**2[b]**	**0**	**4**
Counter/Timers (cont.)	Low Edge Gate Type with Input Debounce Support OLSSC_SUP_GATE_LOW_EDGE_DEBOUNCE Level Change Gate Type with Input Debounce Support OLSSC_SUP_GATE_LEVEL_DEBOUNCE						
Interrupt	Interrupt Support OLSSC_SUP_INTERRUPT						
FIFOs	FIFO in Data Path Support OLSSC_SUP_FIFO						
Processor	Data Processing Capability OLSSC_SUP_PROCESSOR						
Software Calibration	Software Calibration Support OLSSC_SUP_SWCAL						

a. The second D / A subsystem has limited capabilities and is used for threshold triggering only. It has an output range of –10 V to +10 V.

b. DIN and DOUT subsystems use the same DIO lines.

c. All 16 bits of the DIO lines are assigned to A / D input channel 32. While the DIN subsystem itself is incapable of continuous operation, continuous DIN operation can be performed by specifying channel 32 in the channel-gain list of the A / D subsystem and starting the A / D subsystem.

d. The channel-gain list depth of 1024 entries in conjunction with a multiscan of 256 provides an effective channel-gain list depth of up to 256K entries.

e. For DT3016 boards, the maximum retrigger frequency is 166.666 kHz. For DT3010, DT3010-268, DT3010 / 32, DT3010 / 32-268 boards, the maximum retrigger frequency is 357.14 kHz. The maximum retrigger frequency is based on the number of samples per trigger, as follows:

$$\text{Min. Retrigger Period} = \frac{\text{\# of CGL entries} \times \text{\# of CGLs per trigger}}{\text{A / D sample clock frequency}} + 2\ \mu s$$

$$\text{Max. Retrigger Frequency} = \frac{1}{\text{Min. Retrigger Period}}$$

f. The value of 1.2 Hz assumes the minimum number of samples is 1.

g. Channels 0 to 31 are provided for analog input; channel 32 reads all 16 bits from the DIN subsystem.

h. For the DT3016 board only, a filter of 0 kHz or 20 kHz is software-selectable for each DAC.

i. For the DT3010, DT3010-268, DT3010/32, DT3010/32-268 boards, the resolution is 12 bits; for the DT3016 board, the resolution is 16 bits.

j. When configured for 16 bits of resolution, element 0 uses DIO bits 15 to 0 (Banks A and B). When configured for 8 bits of resolution, element 0 uses bits 7 to 0 (Bank A), and element 1 uses bits 15 to 8 (Bank B).

k. OL_TRG_EXTERN is the rising-edge external digital (TTL) trigger input; OL_TRG_EXTRA is the falling-edge digital external (TTL) trigger input.
OL_TRG_THRESHPOS is the rising-edge analog threshold trigger from an analog input channel (for post-trigger acquisition only);
OL_TRG_THRESHNEG is the falling-edge analog threshold trigger from an analog input channel (for post-trigger acquisition only);
OL_TRG_EXTRA+1 is the rising-edge analog input threshold trigger from an external input; and OL_TRG_EXTRA+2 is the falling-edge analog input threshold trigger from an external input.
If you are using an analog threshold trigger for both A/D and D/A subsystems, both triggers must by of the same type (that is, either both must be from an analog input channel or external analog threshold). However, the polarities of the two triggers can be different.

l. For DT3010, DT3010-268, DT3010/32, DT3010/32-268 boards, the maximum A/D throughput is 1.25 MSamples/s. For DT3016 boards, the maximum throughput is 250 kSamples/s.

m. Three conditions are possible:

- 200 kHz per DAC (for the DT3010, DT3010-268, DT3010/32, and DT3010/32-268) or 100 kHz per DAC (for the DT3016) with full-scale steps in continuously-paced or waveform generation mode;
- 500 kHz per DAC (for the DT3010, DT3010-268, DT3010/32, and DT3010/32-268) or 200 kHz per DAC (for the DT3016) with 100 mV steps in waveform generation mode; and
- 500 kHz per DAC (for the DT3010, DT3010-268, DT3010/32, and DT3010/32-268) or 200 kHz per DAC (for the DT3016) with 100 mV steps in continuously-paced mode (system-dependent).

n. If using cascaded timers, this value is 5 MHz.

o. Any two adjacent counter/timers, such as (1,2) or (2,3) or (3,4), can be cascaded in software. If not using cascaded timers, this value is approximately 305.18 Hz.

p. High-edge and low-edge are supported for one-shot and repetitive one-shot modes. High-level and low-level are supported for event counting and rate generation modes.

4

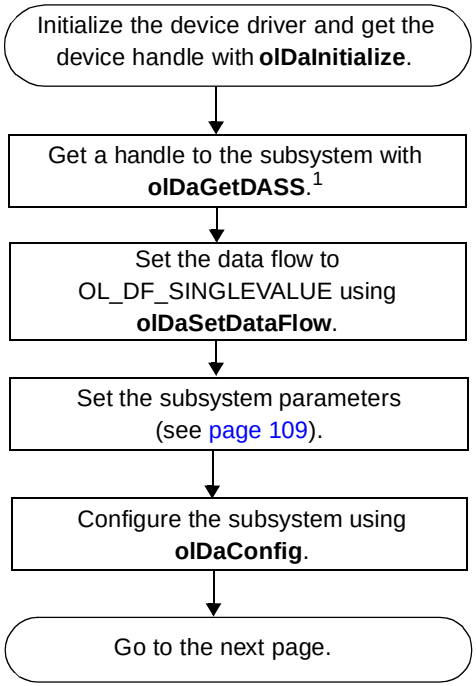
Programming Flowcharts

Single-Value Operations 95
Continuous A/D Operations 97
Continuous D/A Operations 99
Event Counting Operations 101
Frequency Measurement Operations 103
Pulse Output Operations. 105
Simultaneous Operations 107

The following flowcharts show the steps required to perform data acquisition operations using DT-Open Layers. For illustration purposes, the DataAcq SDK functions are shown; however, the concepts apply to all DT-Open Layers software.

Note that many steps represent several substeps; if you are unfamiliar with the detailed operations involved with any one step, refer to the indicated page for detailed information. Optional steps appear in shaded boxes.

Single-Value Operations

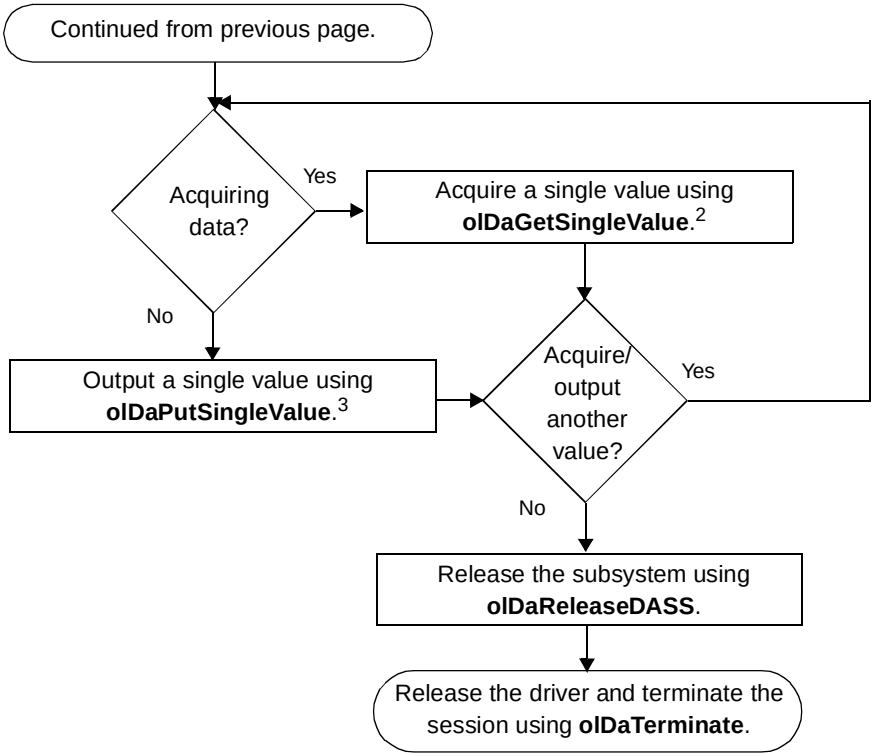

Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the subsystem with **olDaGetDASS**.[1]
Set the data flow to OL_DF_SINGLEVALUE using **olDaSetDataFlow**.
Set the subsystem parameters (see page 109).
Configure the subsystem using **olDaConfig**.
Go to the next page.

Specify A/D for an analog input subsystem, D/A for an analog output subsystem, DIN for a digital input subsystem, or DOUT for a digital output subsystem.

[1] For D/A operations, element 0 contains most of the board's functionality; element 1 is used to set the analog threshold level.

For DIN and DOUT functions, element 0 corresponds to digital port 0 (lines 0 to 7 of Bank A), and element 1 corresponds to digital port 1 (lines 0 to 7 of Bank B).

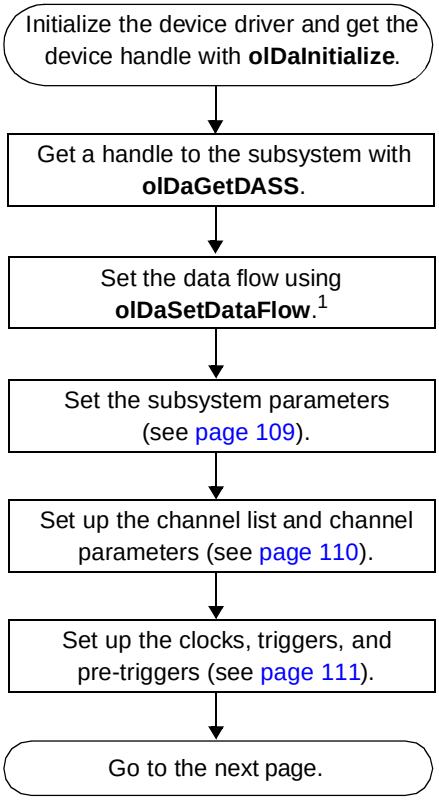
Single-Value Operations (cont.)



[2]For A/D subsystems, read a single analog input value from the specified channel (0 to 31 for single-ended and pseudo-differential configurations or 0 to 15 for the differential configuration) using the specified gain (1, 2, 4, or 8). For DIN subsystems, read the value of the specified digital port.

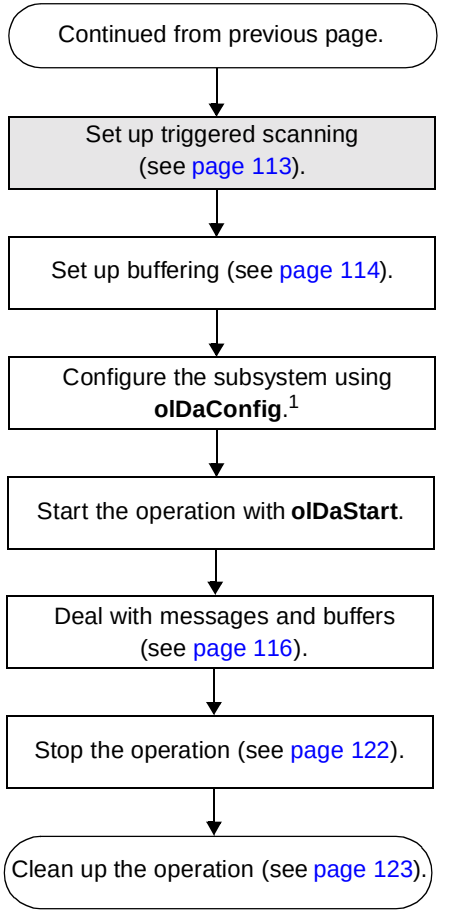
[3] For D/A subsystems, the value is output to the specified channel (DAC 0 or 1) using a gain of 1. For DOUT subsystems, the value is output to the specified digital port.

Continuous A/D Operations


Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the subsystem with **olDaGetDASS**.
Set the data flow using **olDaSetDataFlow**.[1]
Set the subsystem parameters (see page 109).
Set up the channel list and channel parameters (see page 110).
Set up the clocks, triggers, and pre-triggers (see page 111).
Go to the next page.

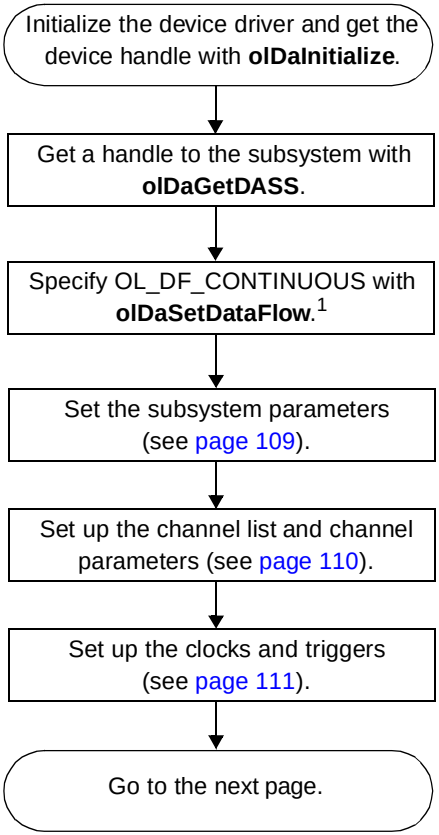
[1] Specify OL_DF_CONTINUOUS (the default value) for normal post-trigger operations, OL_DF_CONTIMNUOUS_PRETRIG for continuous pre-trigger operations, or OL_DF_CONTINUOUS_ABOUTTRIG for continuous about-trigger operations.

Continuous A/D Operations (cont.)


Continued from previous page.
Set up triggered scanning (see page 113).
Set up buffering (see page 114).
Configure the subsystem using olDaConfig.[1]
Start the operation with olDaStart.
Deal with messages and buffers (see page 116).
Stop the operation (see page 122).
Clean up the operation (see page 123).

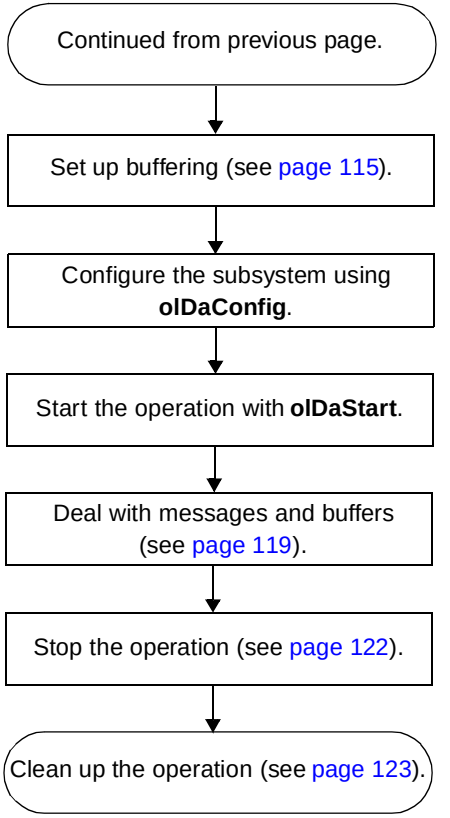
[1] After configuration, if using an internal clock, you can use **olDaGetClockFrequency** to get the actual frequency that the internal pacer clock could achieve; if using internal retrigger mode, you can use **olDaGetRetriggerFrequency** to get the actual frequency that the internal retrigger clock could achieve.

Continuous D/A Operations

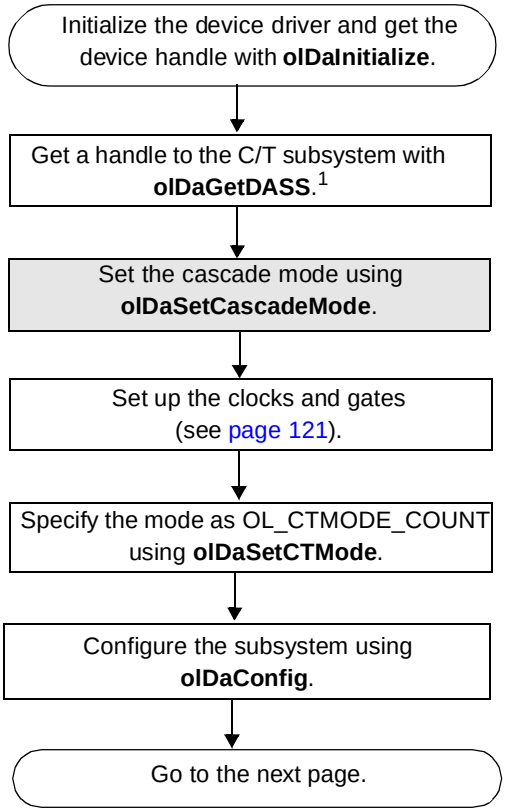

Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the subsystem with **olDaGetDASS**.
Specify OL_DF_CONTINUOUS with **olDaSetDataFlow**.[1]
Set the subsystem parameters (see page 109).
Set up the channel list and channel parameters (see page 110).
Set up the clocks and triggers (see page 111).
Go to the next page.

[1] Continuous mode is the default setting.

Continuous D/A Operations (cont.)

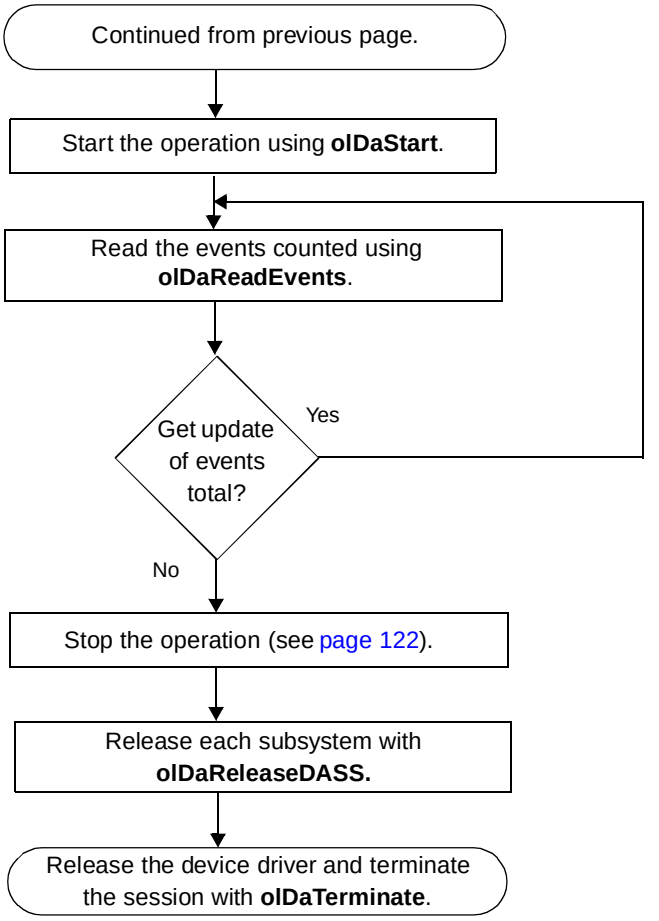

Continued from previous page.
Set up buffering (see page 115).
Configure the subsystem using **olDaConfig**.
Start the operation with **olDaStart**.
Deal with messages and buffers (see page 119).
Stop the operation (see page 122).
Clean up the operation (see page 123).

Event Counting Operations


Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the C/T subsystem with **olDaGetDASS**.[1]
Set the cascade mode using **olDaSetCascadeMode**.
Set up the clocks and gates (see page 121).
Specify the mode as OL_CTMODE_COUNT using **olDaSetCTMode**.
Configure the subsystem using **olDaConfig**.
Go to the next page.

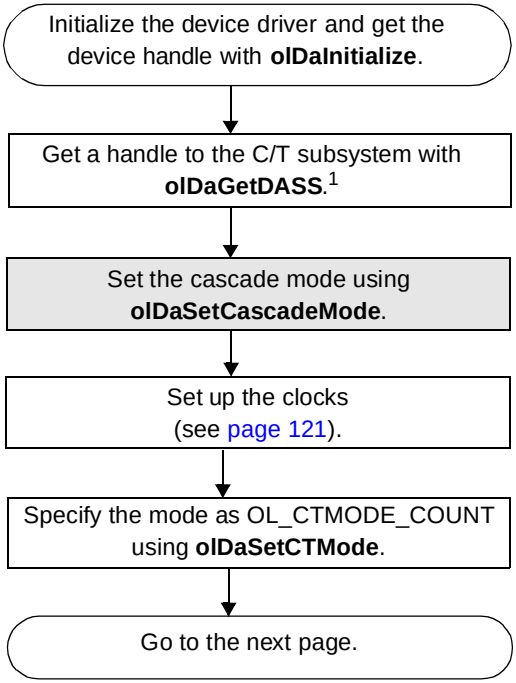
[1] Specify the appropriate C/T subsystem/element. The DT3010 Series supports four elements (0, 1, 2, 3).

Event Counting Operations (cont.)


Continued from previous page.
Start the operation using **olDaStart**.
Read the events counted using **olDaReadEvents**.
Get update of events total?
Yes
No
Stop the operation (see page 122).
Release each subsystem with **olDaReleaseDASS.**
Release the device driver and terminate the session with **olDaTerminate**.

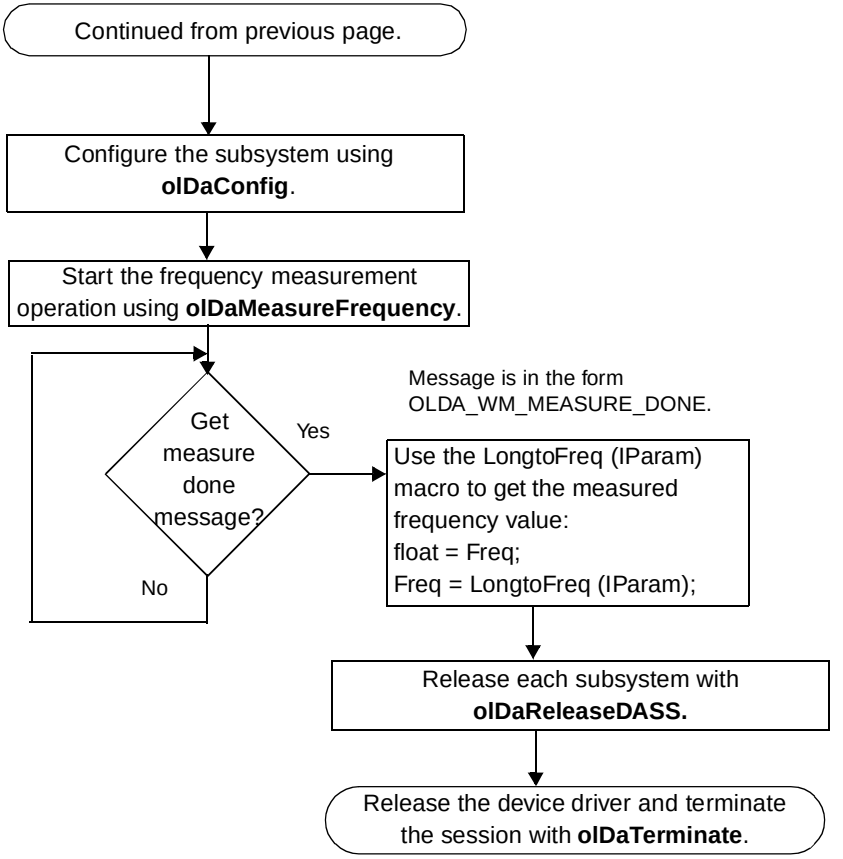
Frequency Measurement Operations

The following flowchart shows the steps required to perform a frequency measurement operation using the system timer with the built-in Windows API function and the functions in the DataAcq SDK. If you need more accuracy the Windows timer provides, refer to the section starting on page 65 of this manual or to your *DataAcq SDK User's Manual* for more information.

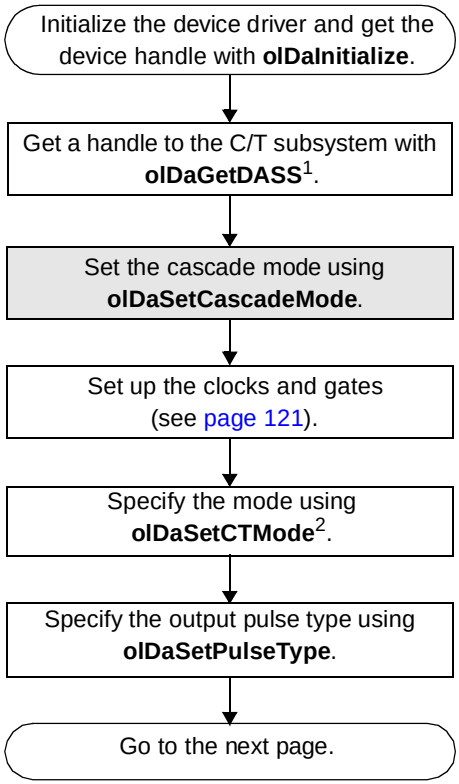

Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the C/T subsystem with **olDaGetDASS**.[1]
Set the cascade mode using **olDaSetCascadeMode**.
Set up the clocks (see page 121).
Specify the mode as OL_CTMODE_COUNT using **olDaSetCTMode**.
Go to the next page.

[1] Specify the appropriate C/T subsystem/element. The DT3010 Series supports four elements (0, 1, 2, 3).

Frequency Measurement Operations (cont.)


Continued from previous page.
Configure the subsystem using **olDaConfig**.
Start the frequency measurement operation using **olDaMeasureFrequency**.
Get measure done message?
Yes
No
Message is in the form OLDA_WM_MEASURE_DONE.
Use the LongtoFreq (IParam) macro to get the measured frequency value:
float = Freq;
Freq = LongtoFreq (IParam);
Release each subsystem with **olDaReleaseDASS.**
Release the device driver and terminate the session with **olDaTerminate**.

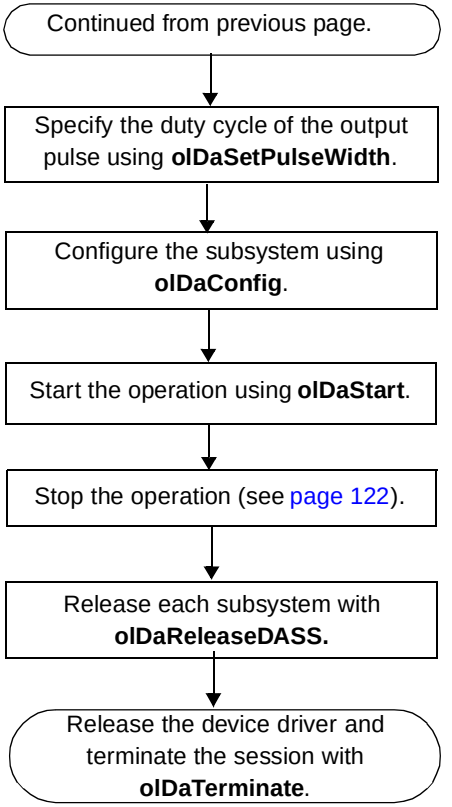
Pulse Output Operations


Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the C/T subsystem with **olDaGetDASS**[1].
Set the cascade mode using **olDaSetCascadeMode**.
Set up the clocks and gates (see page 121).
Specify the mode using **olDaSetCTMode**[2].
Specify the output pulse type using **olDaSetPulseType**.
Go to the next page.

[1] Specify the appropriate C/T subsystem/element. The DT3010 Series supports four elements (0, 1, 2, 3).

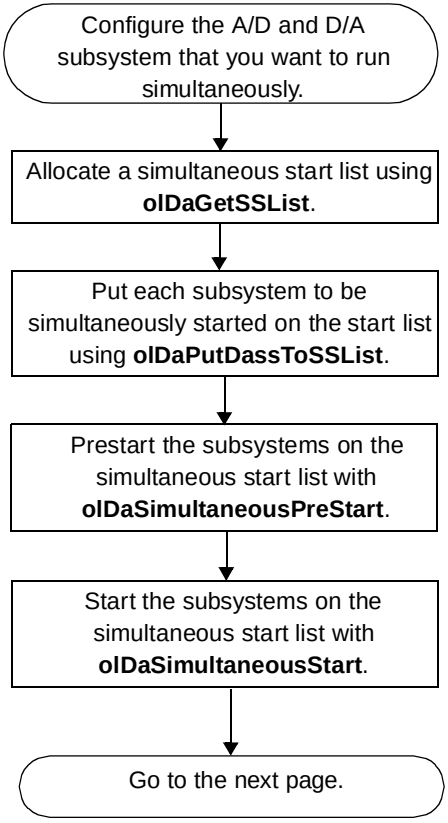
[2] Specify OL_CTMODE_RATE for rate generation (continuous pulse output), OL_CTMODE_ONESHOT for single one-shot, or OL_CTMODE_ONESHOT_RPT for repetitive one-shot.

Pulse Output Operations (cont.)


Continued from previous page.
Specify the duty cycle of the output pulse using **olDaSetPulseWidth**.
Configure the subsystem using **olDaConfig**.
Start the operation using **olDaStart**.
Stop the operation (see page 122).
Release each subsystem with **olDaReleaseDASS.**
Release the device driver and terminate the session with **olDaTerminate**.

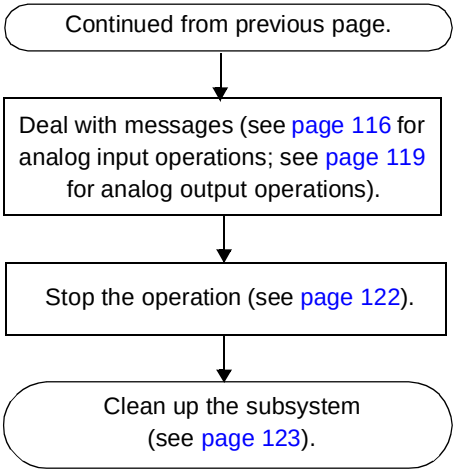
Note that this step is not needed for single one-shot operations.

Simultaneous Operations

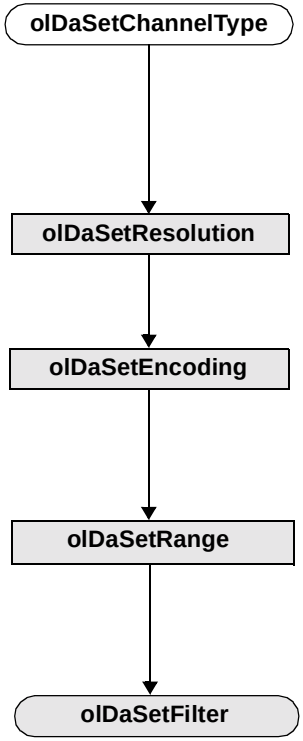

Configure the A/D and D/A subsystem that you want to run simultaneously.
Allocate a simultaneous start list using **olDaGetSSList**.
Put each subsystem to be simultaneously started on the start list using **olDaPutDassToSSList**.
Prestart the subsystems on the simultaneous start list with **olDaSimultaneousPreStart**.
Start the subsystems on the simultaneous start list with **olDaSimultaneousStart**.
Go to the next page.

See the previous flow diagrams in this chapter; note that you cannot perform single-value operations simultaneously.

Simultaneous Operations (cont.)


Continued from previous page.
Deal with messages (see page 116 for analog input operations; see page 119 for analog output operations).
Stop the operation (see page 122).
Clean up the subsystem (see page 123).

Set Subsystem Parameters



Specify the channel type (single-ended or differential – differential is the default). Specify single-ended if you are using pseudo-differential channels (not needed for DIN and DOUT operations).

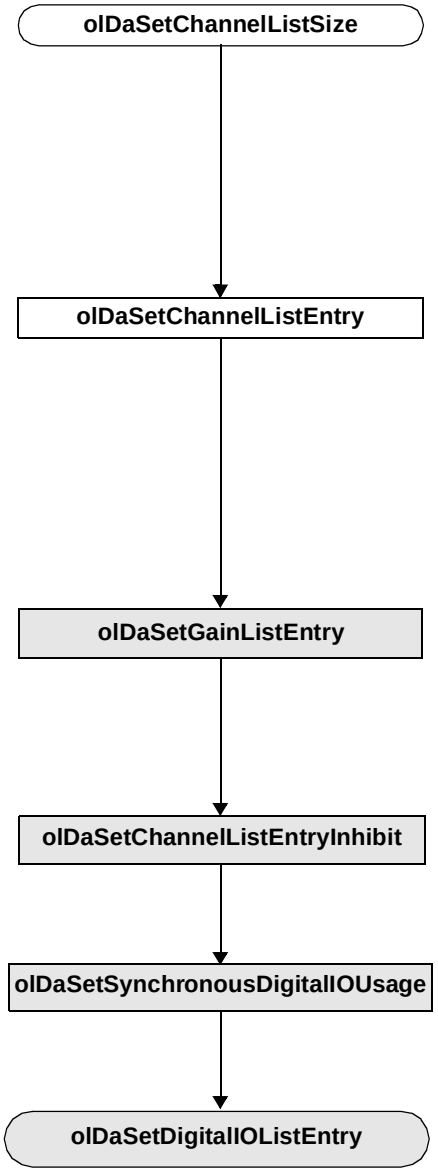
Required only for DIN and DOUT subsystems; specify the resolution as 8 bits (the default) to read port 0 or port 1 only or as 16 to read both ports 0 and 1.

Specify the data encoding type as binary (OL_ENC_BINARY). This is the default value.

Specify the voltage input range for an A/D subsystem (0 to 10 V for unipolar signals or –10 V to +10 V – the default – for bipolar signals). Specify only –10 V to +10 V for D/A subsystems. The step is unnecessary for DIN and DOUT subsystems.

For D/A subsystems only, specify a filter of 20 (20 kHz) for each channel to smooth the output values of the DACs. A filter value of 0 (no filter) is the default value.

Set Up Channel List and Channel Parameters



Specify the size of the analog input or output channel list, gain list, synchronous digital I/O list, and channel-inhibit lists, if applicable (the default is 1).

Set up the analog input or output channel list. For A/D subsystems, when using the single-ended and pseudo-differential configuration, channels 0 to 31 are available; when using the differential configuration, channels 0 to 15 are available. You can enter the digital input channel as channel 32 in the analog input channel list to achieve continuous digital input. If you are using an analog input channel as the threshold trigger, specify the analog input channel used as entry 0 (the default).

For the D/A subsystem, channels 0 and 1 are available.

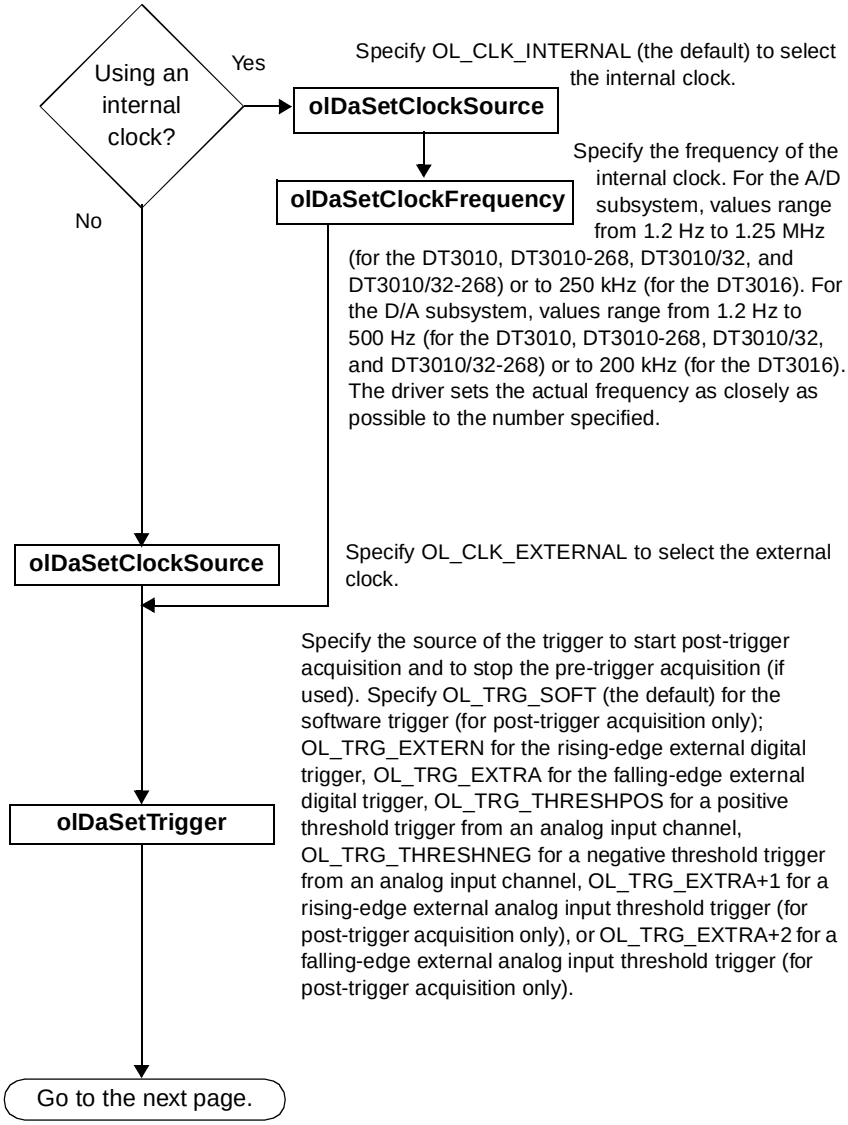
Specify the gain for each channel in the channel list (the gain list parallels the channel list). For A/D subsystems, gains 1,2,4, and 8 are supported; use a gain of 1 (the default) if you use digital channel 32. For D/A subsystems, use a gain of 1.

For A/D subsystems only, enable or disable (the default) inhibition for the specified channel entries. If inhibited, the acquired values from the specified channels are discarded.

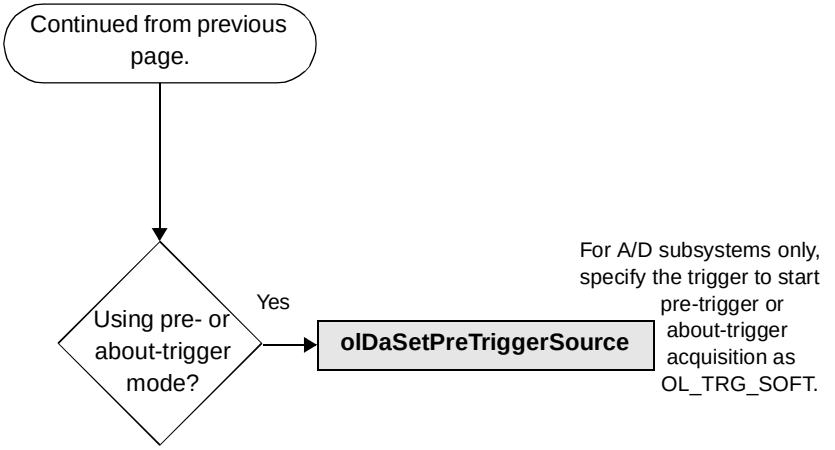
For A/D subsystems only, enable or disable (the default) a synchronous digital output operation

For A/D subsystems only, specify the value to output as each entry in the channel list is sampled. Values range from the default value of 0 (00 in binary format) to 3 (11 in binary format).

Set Clocks, Triggers, and Pre-triggers

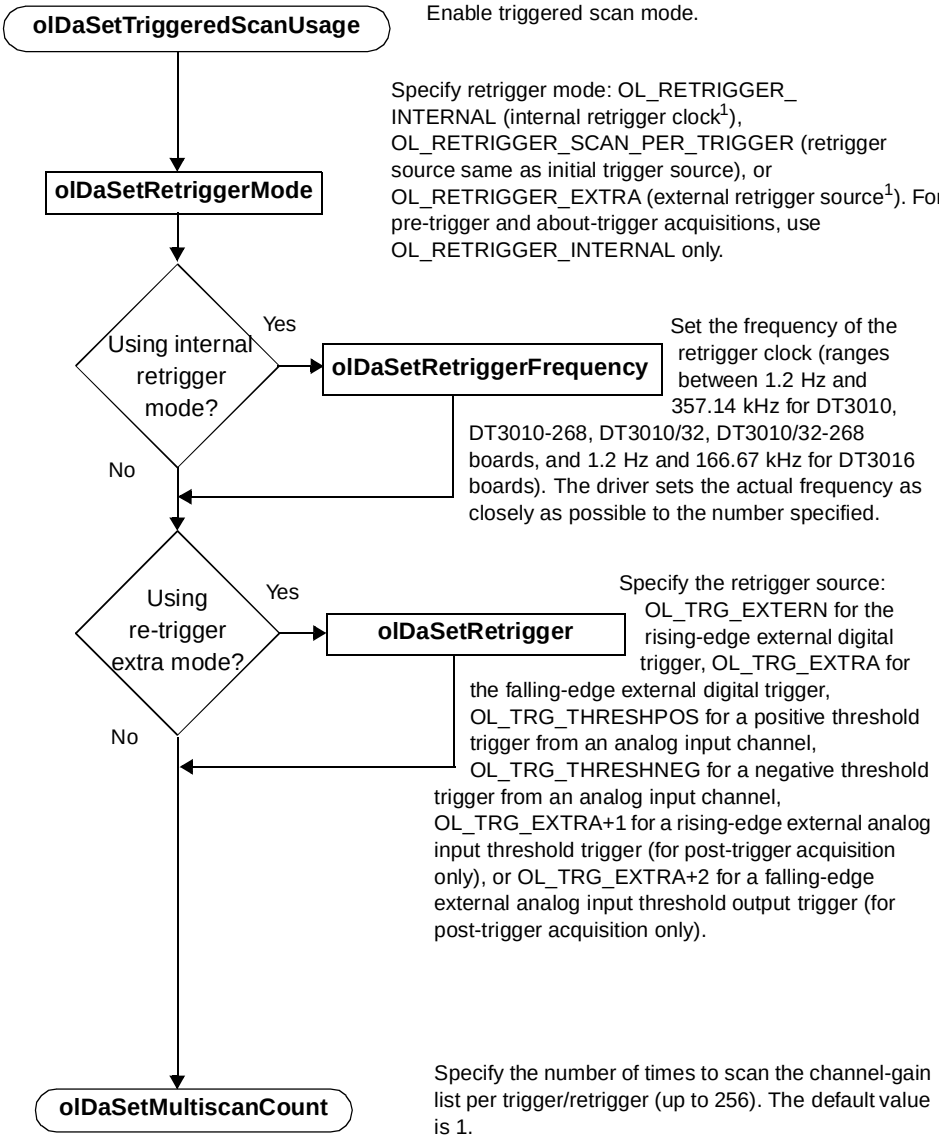

Using an internal clock?
Yes
No
olDaSetClockSource
Specify OL_CLK_INTERNAL (the default) to select the internal clock.
olDaSetClockFrequency
Specify the frequency of the internal clock. For the A/D subsystem, values range from 1.2 Hz to 1.25 MHz (for the DT3010, DT3010-268, DT3010/32, and DT3010/32-268) or to 250 kHz (for the DT3016). For the D/A subsystem, values range from 1.2 Hz to 500 Hz (for the DT3010, DT3010-268, DT3010/32, and DT3010/32-268) or to 200 kHz (for the DT3016). The driver sets the actual frequency as closely as possible to the number specified.
olDaSetClockSource
Specify OL_CLK_EXTERNAL to select the external clock.
olDaSetTrigger
Specify the source of the trigger to start post-trigger acquisition and to stop the pre-trigger acquisition (if used). Specify OL_TRG_SOFT (the default) for the software trigger (for post-trigger acquisition only); OL_TRG_EXTERN for the rising-edge external digital trigger, OL_TRG_EXTRA for the falling-edge external digital trigger, OL_TRG_THRESHPOS for a positive threshold trigger from an analog input channel, OL_TRG_THRESHNEG for a negative threshold trigger from an analog input channel, OL_TRG_EXTRA+1 for a rising-edge external analog input threshold trigger (for post-trigger acquisition only), or OL_TRG_EXTRA+2 for a falling-edge external analog input threshold trigger (for post-trigger acquisition only).
Go to the next page.

Set Clocks, Triggers, and Pre-triggers (cont.)

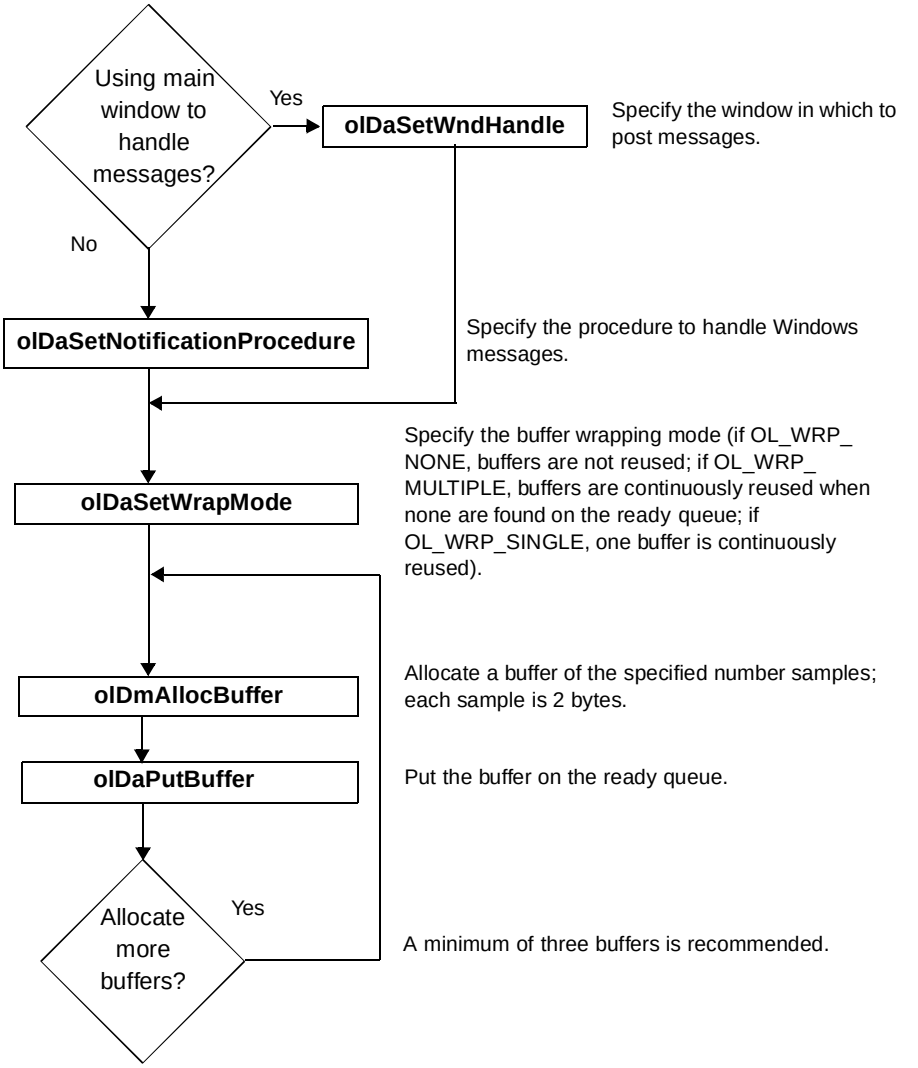

Continued from previous page.
Using pre- or about-trigger mode?
Yes
olDaSetPreTriggerSource
For A/D subsystems only, specify the trigger to start pre-trigger or about-trigger acquisition as OL_TRG_SOFT.

[1] The internal trigger can be set to anything.

Set Up Triggered Scan

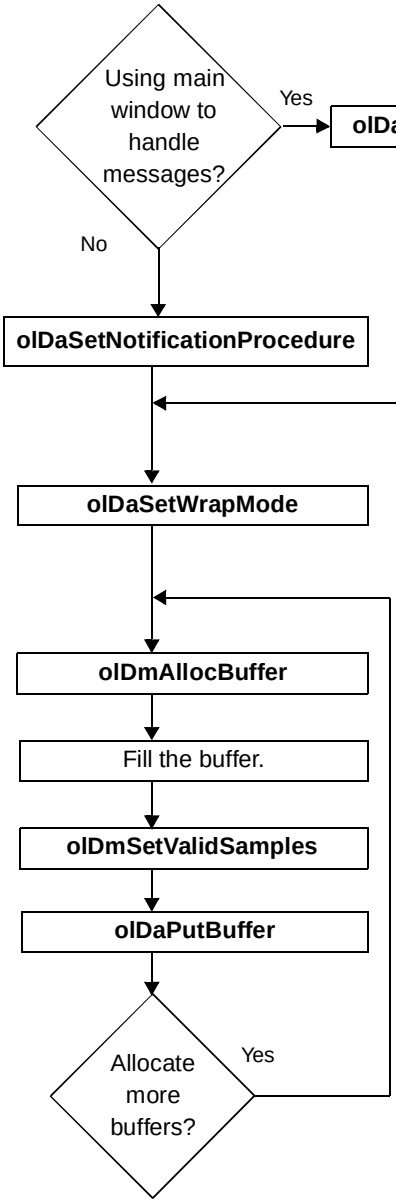

olDaSetTriggeredScanUsage
Enable triggered scan mode.
olDaSetRetriggerMode
Specify retrigger mode: OL_RETRIGGER_INTERNAL (internal retrigger clock[1]), OL_RETRIGGER_SCAN_PER_TRIGGER (retrigger source same as initial trigger source), or OL_RETRIGGER_EXTRA (external retrigger source[1]). For pre-trigger and about-trigger acquisitions, use OL_RETRIGGER_INTERNAL only.
Using internal retrigger mode?
Yes
No
olDaSetRetriggerFrequency
Set the frequency of the retrigger clock (ranges between 1.2 Hz and 357.14 kHz for DT3010, DT3010-268, DT3010/32, DT3010/32-268 boards, and 1.2 Hz and 166.67 kHz for DT3016 boards). The driver sets the actual frequency as closely as possible to the number specified.
Using re-trigger extra mode?
Yes
No
olDaSetRetrigger
Specify the retrigger source: OL_TRG_EXTERN for the rising-edge external digital trigger, OL_TRG_EXTRA for the falling-edge external digital trigger, OL_TRG_THRESHPOS for a positive threshold trigger from an analog input channel, OL_TRG_THRESHNEG for a negative threshold trigger from an analog input channel, OL_TRG_EXTRA+1 for a rising-edge external analog input threshold trigger (for post-trigger acquisition only), or OL_TRG_EXTRA+2 for a falling-edge external analog input threshold output trigger (for post-trigger acquisition only).
olDaSetMultiscanCount
Specify the number of times to scan the channel-gain list per trigger/retrigger (up to 256). The default value is 1.

Set Up A/D Buffering

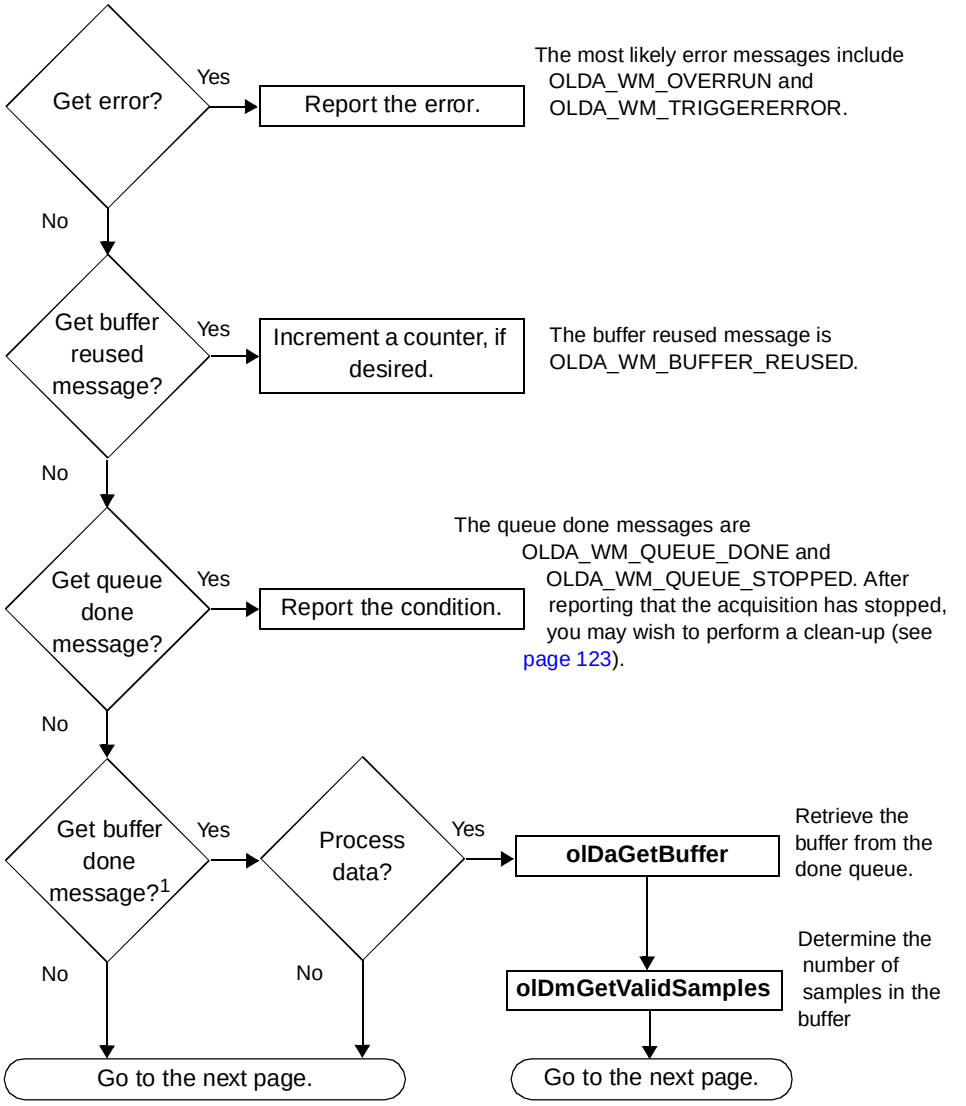

Using main window to handle messages?
Yes
olDaSetWndHandle
Specify the window in which to post messages.
No
olDaSetNotificationProcedure
Specify the procedure to handle Windows messages.
Specify the buffer wrapping mode (if OL_WRP_NONE, buffers are not reused; if OL_WRP_MULTIPLE, buffers are continuously reused when none are found on the ready queue; if OL_WRP_SINGLE, one buffer is continuously reused).
olDaSetWrapMode
olDmAllocBuffer
Allocate a buffer of the specified number samples; each sample is 2 bytes.
olDaPutBuffer
Put the buffer on the ready queue.
Allocate more buffers?
Yes
A minimum of three buffers is recommended.

[1] The buffer done message is OLDA_WM_BUFFER_DONE or OLDA_WM_PRETRIGGER_BUFFER_DONE.

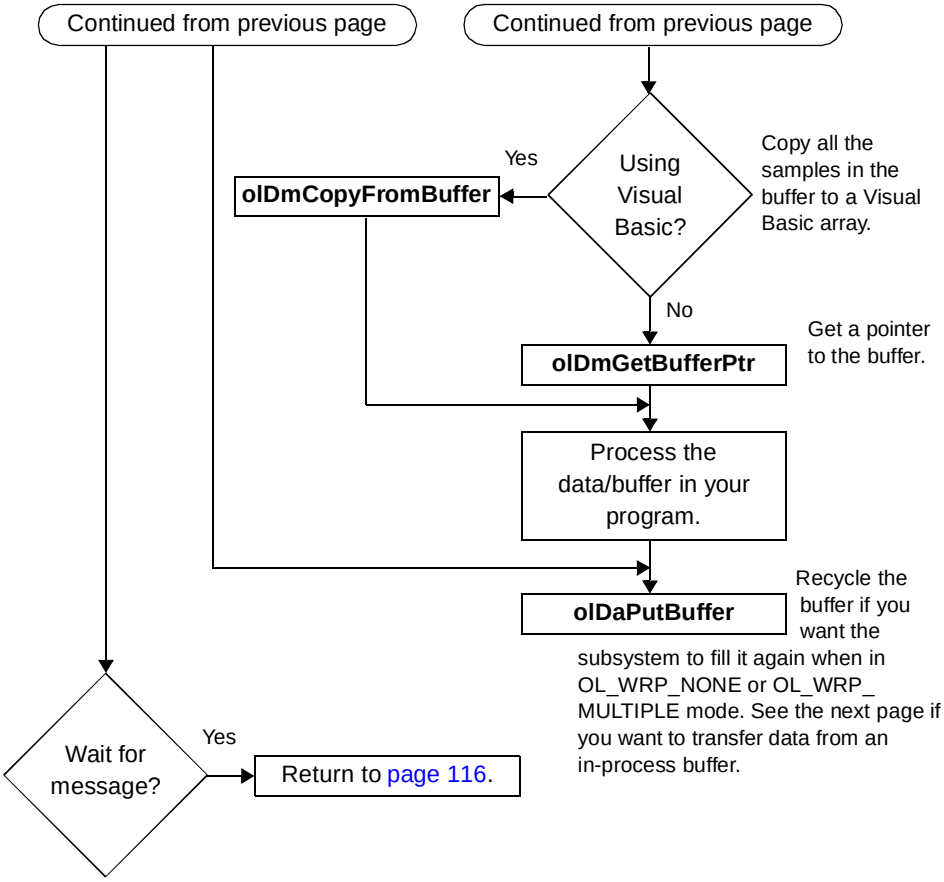
Set Up D/A Buffering


Using main window to handle messages?
Yes
olDaSetWndHandle
Specify the window in which to post messages.
No
olDaSetNotificationProcedure
Specify the procedure to handle Windows messages.
olDaSetWrapMode
Specify the buffer wrapping mode (if OL_WRP_NONE, buffers are not reused; if OL_WRP_MULTIPLE, buffers are continuously reused when none are found on the ready queue; if OL_WRP_SINGLE, one buffer is continuously reused).
olDmAllocBuffer
Allocate a buffer of the specified number samples; each sample is 2 bytes.
Fill the buffer.
Refer to the buffer information starting on page 119 for more information about filling buffers.
olDmSetValidSamples
Specify the valid number of data points in the buffer.
olDaPutBuffer
Put the buffer on the ready queue.
Allocate more buffers?
Yes

Deal with A/D Messages and Buffers

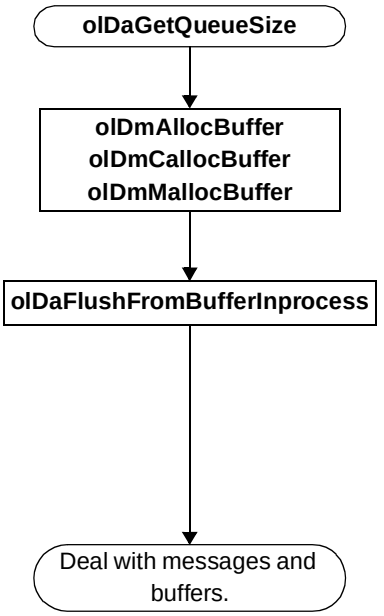


Deal with A/D Messages and Buffers (cont.)


Continued from previous page
Continued from previous page
Using Visual Basic?
Yes
olDmCopyFromBuffer
Copy all the samples in the buffer to a Visual Basic array.
No
olDmGetBufferPtr
Get a pointer to the buffer.
Process the data/buffer in your program.
olDaPutBuffer
Recycle the buffer if you want the subsystem to fill it again when in OL_WRP_NONE or OL_WRP_MULTIPLE mode. See the next page if you want to transfer data from an in-process buffer.
Wait for message?
Yes
Return to page 116.

[1] The buffer done message is OLDA_WM_BUFFER_DONE.

Transfer Data from an Inprocess Buffer



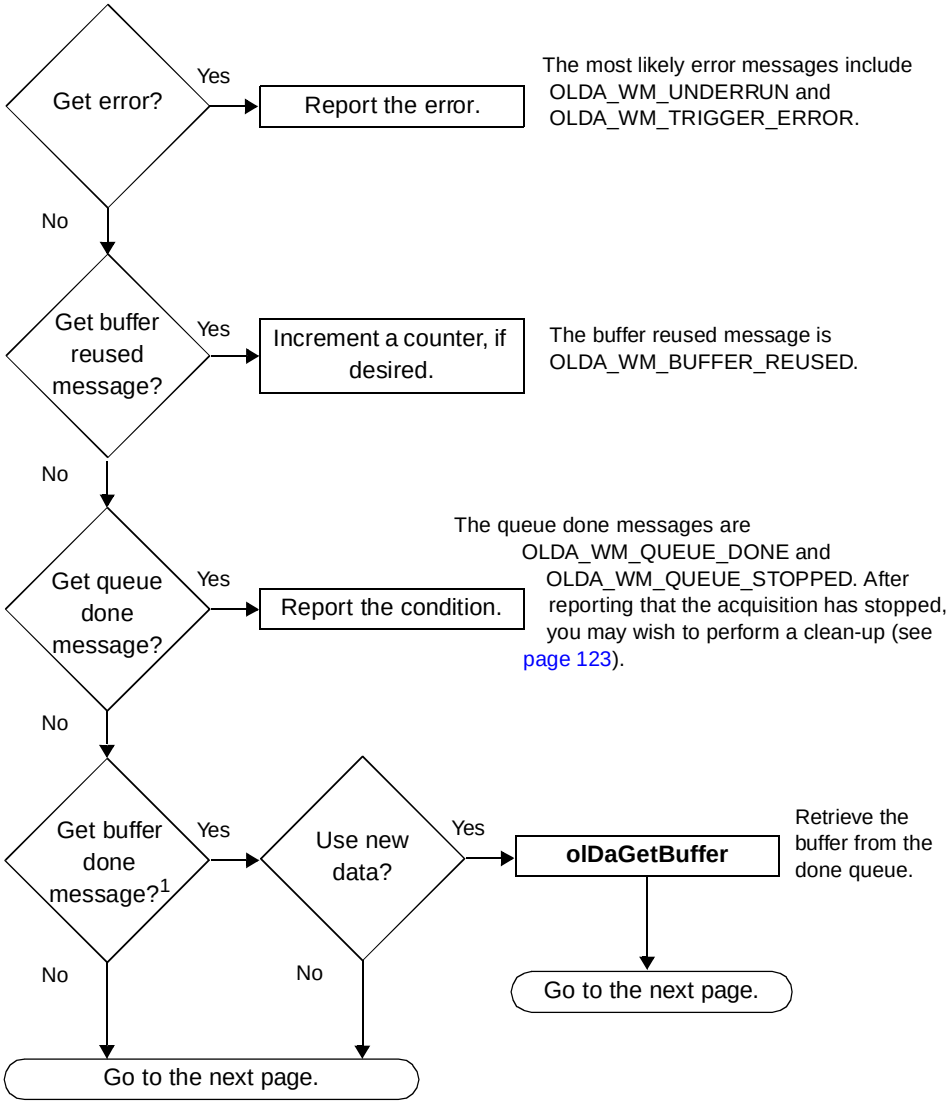
Determine the number of buffers on the inprocess queue (at least one must exist).

Allocate a buffer of the specified number of samples.

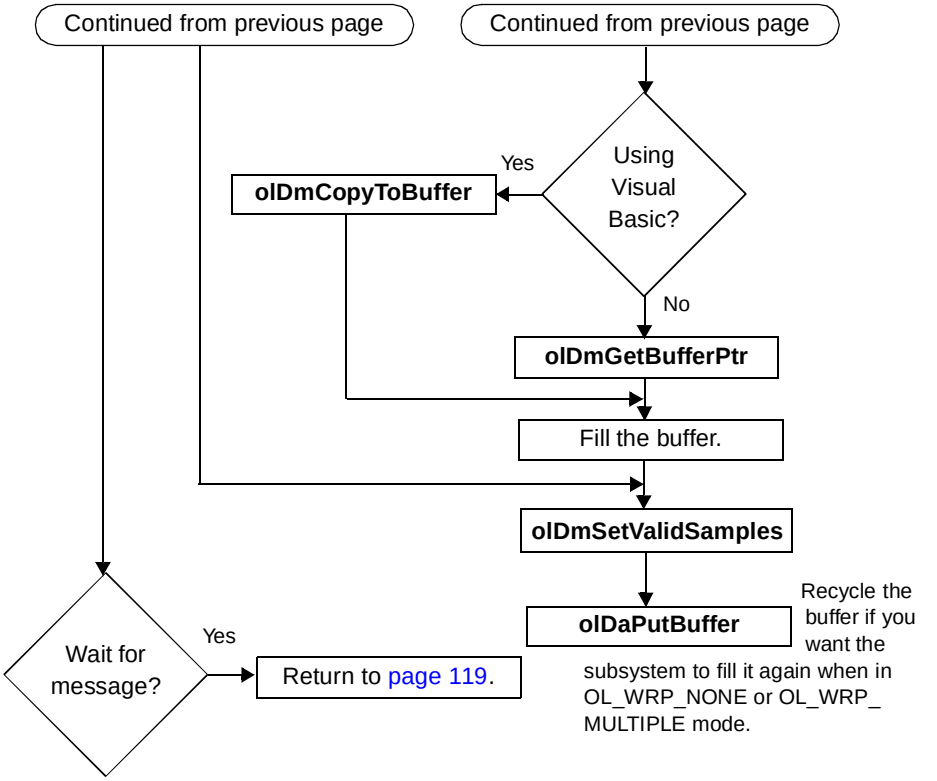
Copy the data from the inprocess buffer to the allocated buffer for immediate processing.

The buffer into which inprocess data was copied was put onto the done queue by the driver, resulting in an OLDA_WM_BUFFER_DONE message. See page 116 for more information.
When the inprocess buffer has been filed, it too is placed on the done queue and an OLDA_WM_BUFFER_DONE message is posted. However, the number of valid samples is equal to the queue's maximum samples minus what was copied out.

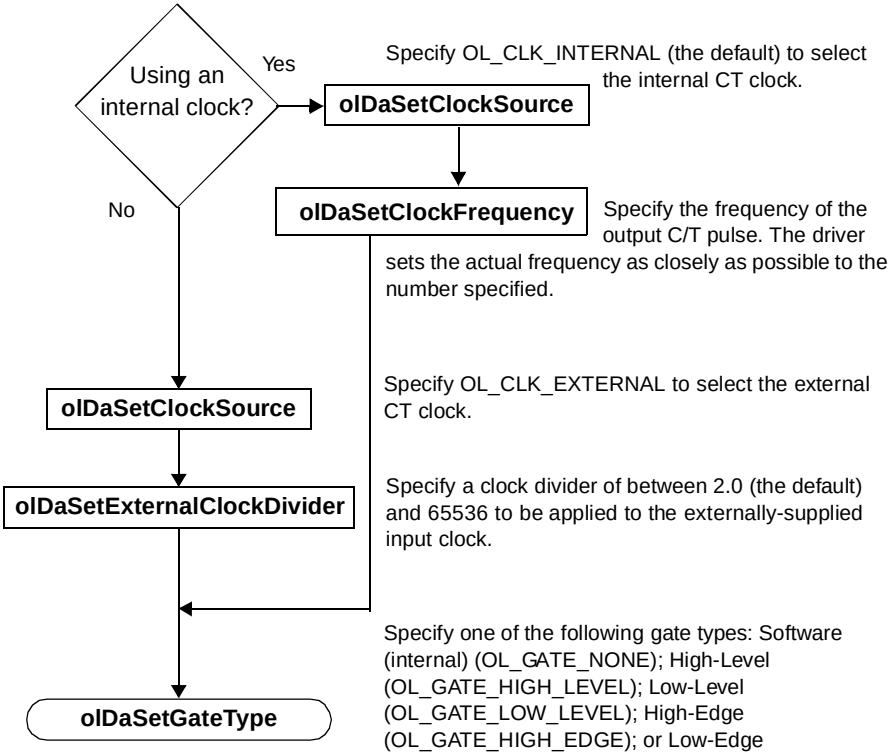
Deal with D/A Messages and Buffers



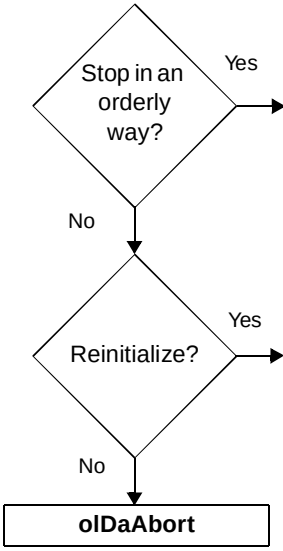
Deal with D/A Messages and Buffers (cont.)



Set Clocks and Gates for Counter/Timer Operations


Using an internal clock?
Yes
No
olDaSetClockSource
Specify OL_CLK_INTERNAL (the default) to select the internal CT clock.
olDaSetClockFrequency
Specify the frequency of the output C/T pulse. The driver sets the actual frequency as closely as possible to the number specified.
olDaSetClockSource
Specify OL_CLK_EXTERNAL to select the external CT clock.
olDaSetExternalClockDivider
Specify a clock divider of between 2.0 (the default) and 65536 to be applied to the externally-supplied input clock.
olDaSetGateType
Specify one of the following gate types: Software (internal) (OL_GATE_NONE); High-Level (OL_GATE_HIGH_LEVEL); Low-Level (OL_GATE_LOW_LEVEL); High-Edge (OL_GATE_HIGH_EDGE); or Low-Edge (OL_GATE_LOW_EDGE).

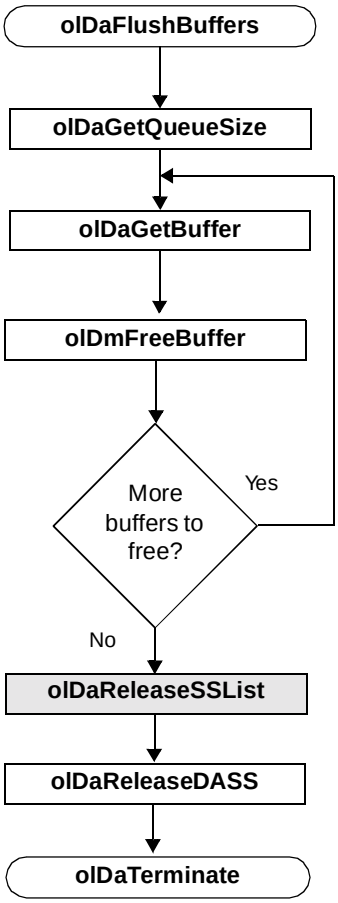
Stop the Operation



olDaStop stops the operation on the subsystem in the orderly way; the current inprocess buffers are filled or emptied and put on the done queue. The driver posts at least one buffer done and queue stopped message.

olDaAbort and **olDaReset** stop the operation on the subsystem immediately; the current buffers are not filled or emptied before they are put on the done queue. **olDaReset** also reinitializes the subsystem to a known state and flushes all buffers to the done queue.

Clean Up the Operation



Flush all buffers on the ready and/or inprocess queues to the done queue.

Determine the number of buffers on the done queue.

Retrieve each buffer on the done queue.

Free each buffer retrieved from the done queue.

For simultaneous operations only, release the simultaneous start list.

Release each subsystem.

Release the device driver and terminate the session.

5

Calibration

Calibrating the Analog Input Subsystem 127
Calibrating the Analog Output Subsystem 141

The DT3010 Series boards are calibrated at the factory and should not require calibration for initial use. It is recommended that you check and, if necessary, readjust the calibration of the analog input and analog output circuitry on the DT3010 Series boards every six months.

The DT3010 Calibration Utility is provided for calibrating the DT3010, DT3010-268, DT3010/32, and DT3010/32-268 boards. The DT3016 Calibration Utility is provided for calibrating the DT3016 board.

Note: Ensure that you installed the DT3010 Series Device Driver and the DT3010 Series Support Software prior to using the DT3010 or DT3016 Calibration Utility. Refer to the *DT3010 Series Getting Started Manual* for more information on installing the device driver and support software.

This chapter describes how to calibrate the analog input and output subsystems of DT3010 Series boards using the DT3010 and DT3016 calibration utilities.

Calibrating the Analog Input Subsystem

This section describes how to configure the DT740, STP268, or STP268-EC screw terminal panel for an internal or external reference, and how to use the DT3010 and DT3016 calibration utilities to calibrate the analog input subsystem of the board.

Choosing a Calibration Reference

To calibrate the analog input circuitry, you can use either of the following references:

- The internal +5 V reference on the DT3010 Series board.

  Using the +5 V reference on the board allows you to calibrate the analog input circuitry quickly without using external equipment; the accuracy of the calibration is approximately 0.05%.

- An external +9.3750 V reference (precision voltage source) available from vendors such as Electronic Development Corporation (EDC).

  Using an external +9.3750 V reference provides an accuracy of approximately ±1 LSB.

This section describes how to configure for an internal or external reference.

Configuring for the Internal Reference

To calibrate the analog input circuitry using the internal +5 V reference, perform the following steps:

1. Connect Analog In 0 to +5 V Reference Out.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Input 0	TB1	TB1 (STP268 must be attached to connector J1)	TB34
+5 V Reference	TB49	TB44 (STP268 must be attached to connector J1)	TB50

2. Connect Analog In 0 Return to Analog Ground.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Input 0 Return	TB2	TB2 (STP268 must be attached to connector J1)	TB68
Analog Ground	TB34	TB34 (STP268 must be attached to connector J1)	TB52

3. Connect Analog In 1 to Analog In 1 Return and Analog Ground.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Input 1	TB2	TB2 (STP268 must be attached to connector J1)	TB33
Analog Input 1 Return	TB4	TB4 (STP268 must be attached to connector J1)	TB67
Analog Ground	TB34	TB34 (STP268 must be attached to connector J1)	TB52

For the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board, follow the instructions on page 131. For the DT3016 board, follow the instructions on page 136.

Configuring for an External Reference

To calibrate the analog input circuitry using an external +9.3750 V reference, perform the following steps:

1. Connect Analog In 0 to the positive side of the precision voltage source.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Input 0	TB1	TB1 (STP268 must be attached to connector J1)	TB34

2. Connect Analog In 0 Return to the negative side of the precision voltage source.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Input 0 Return	TB2	TB2 (STP268 must be attached to connector J1)	TB68

3. Connect Analog In 0 Return to Analog Ground.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Input 0 Return	TB2	TB2 (STP268 must be attached to connector J1)	TB68
Analog Ground	TB34	TB34 (STP268 must be attached to connector J1)	TB52

4. Connect Analog In 1 and Analog In 1 Return to Analog Ground.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Input 1	TB3	TB1 (STP268 must be attached to connector J1)	TB33
Analog Input 1 Return	TB4	TB4 (STP268 must be attached to connector J1)	TB67
Analog Ground	TB34	TB34 (STP268 must be attached to connector J1)	TB52

For the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board, follow the instructions on page 131. For the DT3016 board, follow the instructions on page 136.

Using the DT3010 Calibration Utility

Note: After switching the power on, allow 15 minutes for the board to warm up before calibrating the analog I/O subsystems.

To start the DT3010 Calibration Utility, perform the following steps:

1. Ensure that you installed the DT3010 Series Support Software using the instructions in the *DT3010 Series Getting Started Manual.*
2. Locate the DT3010 Series program folder on your hard disk. This program folder was created when you installed the DT3010 Series Software.

3. Double-click the **DT3010 Calibration Utility** icon in the program folder.
   The main menu appears.

Once the DT3010 Calibration Utility is running and you have connected the required calibration signals to the DT740, STP268, or STP268-EC screw terminal panel, you can calibrate the analog input circuitry of the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board either automatically or manually; auto-calibration is the easiest to use and is the recommended calibration method.

This section describes these calibration methods.

Using the Auto-Calibration Procedure

Auto-calibration is the easiest to use and is the recommended calibration method.

Note: If you want to manually calibrate the bipolar and unipolar ranges instead of auto-calibrating them, refer to "Using the Manual Calibration Procedure" on page 133.

To calibrate the analog input subsystem, perform the following steps:

1. From the main menu of the DT3010 Calibration Utility, click **Configure**, then **Board**.
2. Select the name of the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board to configure from the combo box, then click **OK**.
3. From the main menu of the DT3010 Calibration Utility, click **Calibrate**, then **A/D**.
4. In the Reference Source box, select the reference that you are using (**Internal** or **External**; Internal is the default).

5. In the Auto Calibration box, click **Go**.
   The bipolar (zero and full-scale) and unipolar (zero and full-scale) ranges are automatically calibrated, and the calibration values are displayed. The bipolar readings should be within 0.0049 V; the unipolar readings should be within 0.0024V.
6. Click **OK**.
7. In the Range box, select **PGH Zero**.
8. If the displayed value is not 0.0000 V (within 0.0049 V), continue with "Calibrating the PGH Zero Setting," on page 135; otherwise, click **Quit** when you are finished calibrating the analog input circuitry.

Once you have finished this procedure, continue with "Calibrating the Analog Output Subsystem" on page 141.

Note: If you are not satisfied with the analog input calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the Factory Settings box.

Using the Manual Calibration Procedure

If you want to manually calibrate the analog input circuitry instead of auto-calibrating it, perform the following steps:

1. From the main menu of the DT3010 Calibration Utility, click **Configure**, then **Board**.
2. Select the name of the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board to configure from the combo box, then click **OK**.
3. From the main menu of the DT3010 Calibration Utility, click **Calibrate.**
4. Click **A/D**.

5. In the Reference Source box, select the reference that you are using (**Internal** or **External**; Internal is the default).
6. In the Range box, select **Bipolar**, then **Zero**.
7. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 0.0000 V (within 0.0049 V).
8. In the Range box, select **Bipolar**, then **+FS** (for full-scale).
9. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 5 V with the internal reference or +9.3750 V with the external reference (within 0.0049 V).
10. In the Range box, select **Unipolar**, then **Zero**.
11. Click the increment or decrement arrows in the Manual Adjustment box until the display reads just above 0 V, then use the decrement arrow until the first value of 0 V is displayed (within 0.0024 V).
12. In the Range box, select **Unipolar**, then **+FS** (for full-scale).
13. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 5 V with the internal reference or +9.3750 V with the external reference (within 0.0024 V).
14. In the Range box, select **PGH Zero**.
15. If the displayed value is not 0.0000 V (within 0.0049 V), perform the procedure in the next; otherwise, click **Quit** when you are finished calibrating the analog input circuitry.

Once you have finished this procedure, continue with "Calibrating the Analog Output Subsystem" on page 141.

Note: If you are not satisfied with the analog input calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the Factory Settings box.

Calibrating the PGH Zero Setting

PGH Zero is a factory-calibrated setting and, generally, should not need adjustment. However, if you select **PGH Zero** in the Range box and a value other than 0.0000 V is displayed, perform the following steps to calibrate this setting:

1. In the Range box, select **PGH Zero**.
2. Physically adjust potentiometer R4 on the DT3010/32 or DT3010/32-268 board until the display reads 0.0000 V (within 0.0049 V for the DT3010, DT3010/32, and DT3010/32-268). Figure 24 shows the location of this potentiometer.

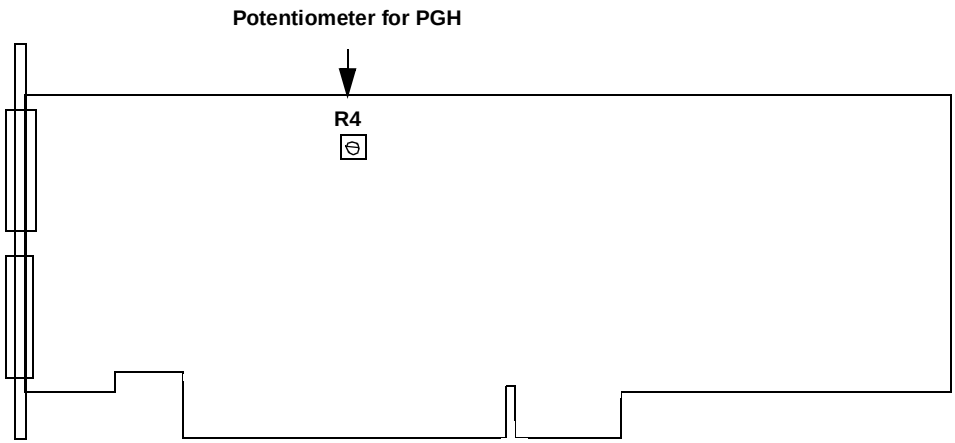


Figure 24: Location of Potentiometer R4 on the DT3010, DT3010-268, DT3010/32, and DT3010/32-268 Boards

3. Click **Quit** when you are finished.

Once you have finished this procedure, continue with "Calibrating the Analog Output Subsystem" on page 141.

Using the DT3016 Calibration Utility

Note: After switching the power on, allow 15 minutes for the board to warm up before calibrating the analog I/O subsystems.

To start the DT3016 Calibration Utility, perform the following steps:

1. Ensure that you installed the DT3010 Series Support Software using the instructions in the *DT3010 Series Getting Started Manual.*
2. Locate the DT3010 Series program folder on your hard disk. This program folder was created when you installed the DT3010 Series Support Software.
3. Double-click the **DT3016 Calibration Utility** icon in the program folder.
   The main menu appears.

Once the DT3016 Calibration Utility is running and you have connected the required calibration signals to the DT740 screw terminal panel, you can calibrate the analog input circuitry of the DT3016 board either automatically or manually; auto-calibration is the easiest to use and is the recommended calibration method.

This section describes these calibration methods.

Using the Auto-Calibration Procedure

Auto-calibration is the easiest to use and is the recommended calibration method.

Note: If you want to manually calibrate the bipolar and unipolar ranges instead of auto-calibrating them, refer to "Using the Manual Calibration Procedure" on page 138.

To calibrate the analog input subsystem, perform the following steps:

1. From the main menu of the DT3016 Calibration Utility, click **Configure**, then **Board**.
2. Select the name of the DT3016 board to configure from the combo box, then click **OK**.
3. From the main menu of the DT3016 Calibration Utility, click **Calibrate**, then **A/D**.
4. In the Reference Source box, select the reference that you are using (**Internal** or **External**; Internal is the default).
5. In the Auto Calibration box, click **Go**.
   The bipolar (zero and full-scale) and unipolar (zero and full-scale) ranges are automatically calibrated, and the calibration values are displayed. The bipolar readings should be within 0.001 V; the unipolar readings should be within 0.0005V.
6. Click **OK**.
7. In the Range box, select **PGH Zero**.
8. If the displayed value is not 0.0000 V (within 0.001 V), continue with "Calibrating the PGH Zero Setting" on page 139; otherwise, click **Quit** when you are finished calibrating the analog input circuitry.

Once you have finished this procedure, continue with "Calibrating the Analog Output Subsystem" on page 141.

Note: If you are not satisfied with the analog input calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the Factory Settings box.

Using the Manual Calibration Procedure

If you want to manually calibrate the analog input circuitry instead of auto-calibrating it, perform the following steps:

1. From the main menu of the DT3016 Calibration Utility, click **Configure**, then **Board**.
2. Select the name of the DT3016 board to configure from the combo box, then click **OK**.
3. From the main menu of the DT3016 Calibration Utility, click **Calibrate.**
4. Click **A/D**.
5. In the Reference Source box, select the reference that you are using (**Internal** or **External**; Internal is the default).
6. In the Range box, select **Bipolar**, then **Zero**.
7. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 0.0000 V (within 0.001 V).
8. In the Range box, select **Bipolar**, then **+FS** (for full-scale).
9. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 5 V with the internal reference or +9.3750 V with the external reference (within 0.001 V).
10. In the Range box, select **Unipolar**, then **+FS** (for full-scale).
11. Click the increment or decrement arrows in the Manual Adjustment box until the display reads 5 V with the internal reference or +9.3750 V with the external reference (within 0.0005 V).

12. In the Range box, select **Unipolar**, then **Zero**.
13. Click the increment or decrement arrows in the Manual Adjustment box until the display reads just above 0 V, then use the decrement arrow until the first value of 0 V is displayed (within 0.0005 V).
14. In the Range box, select **PGH Zero**.
15. If the displayed value is not 0.0000 V (within 0.001 V), perform the procedure in the next section; otherwise, click **Quit** when you are finished calibrating the analog input circuitry.

Once you have finished this procedure, continue with "Calibrating the Analog Output Subsystem" on page 141.

Note: If you are not satisfied with the analog input calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the Factory Settings box.

Calibrating the PGH Zero Setting

PGH Zero is a factory-calibrated setting and, generally, should not need adjustment. However, if you select **PGH Zero** in the Range box and a value other than 0.0000 V is displayed, perform the following steps to calibrate this setting:

1. In the Range box, select **PGH Zero**.
2. Physically adjust potentiometer R2 on the DT3016 until the display reads 0.0000 V (0.001 V). Figure 25 shows the location of this potentiometer.

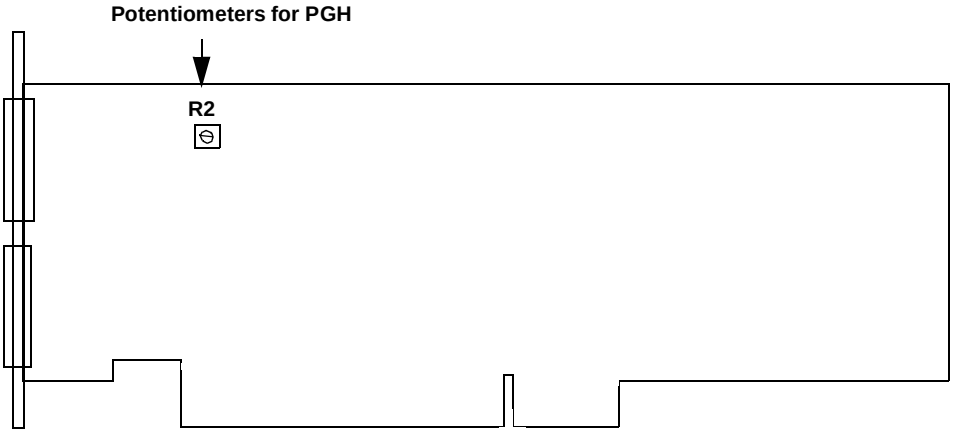


Figure 25: Location of Potentiometer R2 on the DT3016 Board

3. Click **Quit** when you are finished.

Once you have finished this procedure, continue with the next section.

Calibrating the Analog Output Subsystem

This section describes how to configure the DT740, STP268, or STP268-EC screw terminal panel for an internal or external meter, and how to use the DT3010 and DT3016 calibration utilities to calibrate the analog output subsystems of the board.

Choosing a Calibration Meter

To calibrate the analog output circuitry, you can use either of the following meters:

- The internal A/D converter (ADC) on the DT3010 Series board.

  Using the board's ADC as an input to the analog output circuitry allows you to calibrate the analog output circuitry quickly without using external equipment.

- An external precision meter available from vendors, such as Fluke.

The following sections describe how to configure for calibration using either of the supported meters.

Configuring for the Internal ADC

To calibrate DAC0 using the internal ADC, perform the following steps:

1. Connect Analog Out 0+ (TB41) to Analog In 2 (TB5).

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Output 0+	TB41	TB41 (STP268 must be attached to connector J1)	TB17
Analog Input 2	TB5	TB5 (STP268 must be attached to connector J1)	TB32

2. Connect Analog Out Return to Analog In 2 Return.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Output Return	TB42	TB42 (STP268 must be attached to connector J1)	TB51
Analog Input 2 Return	TB6	TB6 (STP268 must be attached to connector J1)	TB66

To calibrate DAC1 using the internal ADC, perform the following steps:

1. Connect Analog Out 1+ to Analog In 3.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Output 1+	TB43	TB43 (STP268 must be attached to connector J1)	TB16
Analog Input 3	TB7	TB7 (STP268 must be attached to connector J1)	TB31

2. Connect Analog Out Return to Analog In 3 Return.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Output 1+ Return	TB44	TB42 (STP268 must be attached to connector J1)	TB51
Analog Input 3 Return	TB8	TB8 (STP268 must be attached to connector J1)	TB65

For the DT3010, DT3010-268, DT3010/32, DT3010/32-268 board, follow the instructions on page 146. For the DT3016 board, follow the instructions on page 148.

Configuring for an External Meter

To calibrate DAC0 using an external voltage meter, perform the following steps:

1. Connect Analog Out 0+ to the positive side of the precision voltage meter.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Output 0+	TB41	TB41 (STP268 must be attached to connector J1)	TB17

2. Connect Analog Out 0 Return to the negative side of the precision voltage meter.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Output 0 Return	TB42	TB42 (STP268 must be attached to connector J1)	TB51

To calibrate DAC1 using an external voltage meter, perform the following steps:

1. Connect Analog Out 1+ to the positive side of the precision voltage meter.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Output 1+	TB43	TB43 (STP268 must be attached to connector J1)	TB16

2. Connect Analog Out 1 Return (TB44) to the negative side of the precision voltage meter.

Signal	DT740 Screw Terminal	STP268 Screw Terminal	STP268-EC Screw Terminal
Analog Output 1+ Return	TB44	TB42 (STP268 must be attached to connector J1)	TB51

For the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board, follow the instructions on page 146. For the DT3016 board, follow the instructions on page 148.

Using the DT3010 Calibration Utility

Once the DT3010 Calibration Utility is running and you have connected the required calibration signals to the DT740, STP268, or STP268-EC screw terminal panel, perform the following steps to calibrate the analog output subsystem on the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board:

1. From the main menu of the DT3010 Calibration Utility, click **Configure**, then **Board**.
2. Select the name of the DT3010, DT3010-268, DT3010/32, DT3010/32-268 board to configure from the combo box, then click **OK**.
3. From the main menu of the DT3010 Calibration Utility, click **Calibrate**, then **D/A**.
4. In the Meter Selection box, select the meter that you are using (**Internal** or **External**; Internal is the default).
5. In the Mode box, select **Calibrate**.
6. In the D/A box, select **DAC 0**.
7. In the Voltages box, select **–9.3750**.
8. Physically adjust potentiometer R15 on the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board until the display reads –9.3750 V (within 0.001 V). Figure 26 shows the location of this potentiometer.

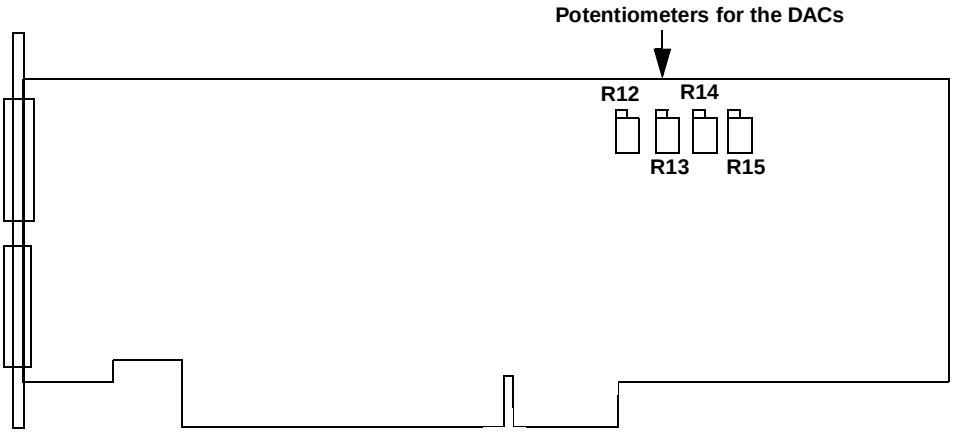


Figure 26: Location of Potentiometers R12 to R15 on the DT3010, DT3010-268, DT3010/32, and DT3010/32-268

9. In the Voltages box, select +**9.3750**.
10. Physically adjust potentiometer R14 on the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board until the display reads +9.3750 V (within 0.001 V). Figure 26 shows the location of this potentiometer.
11. In the D/A box, select **DAC 1**.
12. In the Voltages box, select –**9.3750**.
13. Physically adjust potentiometer R13 on the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board until the display reads –9.3750 V (within 0.001 V). Figure 26 shows the location of this potentiometer.
14. In the Voltages box, select +**9.3750**.
15. Physically adjust potentiometer R12 on the DT3010, DT3010-268, DT3010/32, or DT3010/32-268 board until the display reads

+9.3750 V (within 0.001 V). Figure 26 shows the location of this potentiometer.

Note: If you want to check the values for intermediate ranges, select **Display Values** in the Mode box and select any of the available ranges; the range is then displayed. *You cannot calibrate intermediate ranges*.

---

16. Click **Quit** when you are finished calibrating the analog output circuitry.

Once you have finished this procedure, the analog output circuitry is calibrated. To close the DT3010 Calibration Utility, click the close box in the upper, right corner of the window.

Using the DT3016 Calibration Utility

Once the DT3016 Calibration Utility is running and you have connected the required calibration signals to the DT740 screw terminal panel, perform the following steps to calibrate the analog output subsystem on the DT3016 board:

1. From the main menu of the DT3016 Calibration Utility, click **Configure**, then **Board**.
2. Select the name of the DT3016 board to configure from the combo box, then click **OK**.
3. From the main menu of the DT3016 Calibration Utility, click **Calibrate**, then **D/A**.
4. In the Meter Selection box, select the meter that you are using (**Internal** or **External**; Internal is the default).
5. In the Mode box, select **Calibrate**.
6. In the D/A box, select **DAC 0**.
7. In the Voltages box, select **–9.3750**.

8. Physically adjust potentiometer R15 on the DT3016 board until the display reads –9.3750 V (within 0.001 V). Figure 27 shows the location of this potentiometer.

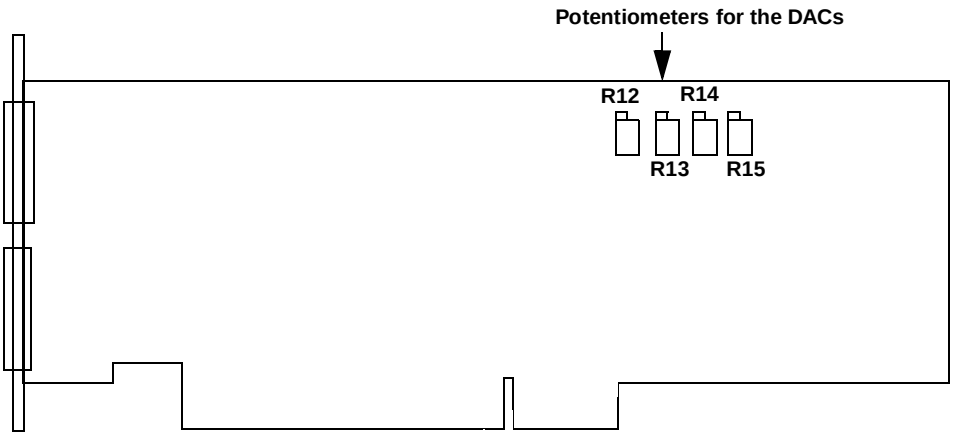


Figure 27: Location of Potentiometers R12 to R15 on the DT3016 Board

9. In the Voltages box, select +**9.3750**.
10. Physically adjust potentiometer R14 on the DT3016 board until the display reads +9.3750 V (within 0.001 V). Figure 27 shows the location of this potentiometer.
11. In the D/A box, select **DAC 1**.
12. In the Voltages box, select –**9.3750**.
13. Physically adjust potentiometer R13 on the DT3016 board until the display reads –9.3750 V (within 0.001 V). Figure 27 shows the location of this potentiometer.
14. In the Voltages box, select +**9.3750**.

15. Physically adjust potentiometer R12 on the DT3016 board until the display reads +9.3750 V (within 0.001 V). Figure 27 shows the location of this potentiometer.

Note: If you want to check the values for intermediate ranges, select **Display Values** in the Mode box and select any of the available ranges; the range is then displayed. *You cannot calibrate intermediate ranges*.

---

16. Click **Quit** when you are finished calibrating the analog output circuitry.

Once you have finished this procedure, the analog output circuitry is calibrated. To close the DT3016 Calibration Utility, click the close box in the upper, right corner of the window.

6

Troubleshooting

Service and Support 155
If Your Board Needs Factory Service 159

General Checklist

Should you experience problems using the DT3010 Series board, please follow these steps:

1. Read all the documentation provided for your product. Make sure that you have added any "Read This First" information to your manual and that you have used this information.
2. Check the Data Acquisition OMNI CD for any README files and ensure that you have used the latest installation and configuration information available.
3. Check that your system meets the requirements stated in the *DT3010 Series Getting Started Manual.*
4. Check that you have installed your hardware properly using the instructions in the *DT3010 Series Getting Started Manual.*
5. Check that you have installed and configured the device driver properly using the instructions in the *DT3010 Series Getting Started Manual.*
6. Search the DT Knowledgebase in the Support section of the Data Translation web site (at www.datatranslation.com) for an answer to your problem.

If you still experience problems, try using the information in Table 7 to isolate and solve the problem. If you cannot identify the problem, refer to "Service and Support," starting on page 155.

Table 7: Troubleshooting Problems

Symptom	Possible Cause	Possible Solution
Board does not respond.	The board configuration is incorrect.	Check the configuration of your device driver to ensure that the board name and type are correct; see the instructions starting in the *DT3010 Series Getting Started Manual*.
	The board is incorrectly aligned in a PCI expansion slot.	Check that the slot in which your DT3010 Series board is located is a PCI slot and that the board is correctly seated in the slot; see the instructions in the *DT3010 Series Getting Started Manual*.
	The board is damaged.	Contact Data Translation for technical support; refer to page 155.
Intermittent operation.	Loose connections or vibrations exist.	Check your wiring and tighten any loose connections or cushion vibration sources; see the instructions in the *DT3010 Series Getting Started Manual*.
	The board is overheating.	Check environmental and ambient temperature; consult the board's specifications on page 172 of this manual and the documentation provided by your computer manufacturer for more information.
	Electrical noise exists.	Check your wiring and either provide better shielding or reroute unshielded wiring; see the instructions in the *DT3010 Series Getting Started Manual*.

Table 7: Troubleshooting Problems (cont.)

Symptom	Possible Cause	Possible Solution
Data appears to be invalid.	An open connection exists.	Check your wiring and fix any open connections; see the instructions in the *DT3010 Series Getting Started Manual*.
	A transducer is not connected to the channel being read.	Check the transducer connections; see the instructions in the *DT3010 Series Getting Started Manual*.
	The board is set up for differential inputs while the transducers are wired as single-ended inputs or vice versa.	Check your wiring and ensure that what you specify in software matches your hardware configuration; see the instructions in the *DT3010 Series Getting Started Manual.*
Computer does not boot.	Board is not seated properly.	Check that the slot in which your DT3010 Series board is located is a PCI slot, that the board is correctly seated in the slot, and that the board is secured in the slot with a screw; see the instructions in the *DT3010 Series Getting Started Manual.*
	The power supply of the computer is too small to handle all the system resources.	Check the power requirements of your system resources and, if needed, get a larger power supply; consult the board's specifications on page 172 of this manual.
System lockup.	Board is not seated properly.	Check that the slot in which your DT3010 Series board is located is a PCI slot, that the board is correctly seated in the slot, and that the board is secured in the slot with a screw; see the instructions in the *DT3010 Series Getting Started Manual.*

Service and Support

If you have difficulty using the DT3010 Series board, Data Translation's Technical Support Department is available to provide prompt technical assistance. Support upgrades, technical information, and software are also available.

All customers can always obtain the support needed. The first 90 days are complimentary, as part of the product's original warranty, to help you get your system running. Customers who call outside of this time frame can either purchase a support contract or pay a nominal fee (charged on a per-incident basis).

For "priority support," purchase a support contract. Support contracts guarantee prompt response and are very affordable; contact your local sales office for details.

Refer to the Data Translation Support Policy located at the end of this manual for a list of services included and excluded in our standard support offering.

Telephone Technical Support

Telephone support is normally reserved for original warranty and support-contract customers. Support requests from non-contract or out-of-warranty customers are processed after requests from original warranty and support-contract customers.

For the most efficient service, please complete the form on page 157 and be at your computer when you call for technical support. This information helps to identify specific system and configuration-related problems and to replicate the problem in house, if necessary.

You can reach the Technical Support Department by calling (508) 481-3700 x1401.

If you are located outside the USA, call your local distributor. The name and telephone number of you nearest distributor are provided in your Data Translation catalog.

If you are leaving a message to request a support call, please include the following information:

- Your name (please include proper spelling),
- Your company or organization (please include proper spelling),
- A phone number,
- An email address where you can be reached,
- The hardware / software product you need help on,
- A summary of the issue or question you have,
- Your contract number, if applicable, and
- Your product serial number or purchase date.

Omitting any of the above information may delay our ability to resolve your issue.

Information Required for Technical Support

Name:_____Phone_____
Contract Number: _____
Address: _____
_____

Data Translation hardware product(s): _____
serial number: _____
configuration: _____
Data Translation device driver - SPO number: _____ _____
version: _____
Data Translation software - SPO number: _____ _____
serial number: _____ version: _____
PC make/model: _____
operating system: _____ version: _____
Windows version: _____
processor: _____ speed: _____
RAM: _____ hard disk space: _____
network/number of users: _____ disk cache: _____
graphics adapter: _____ data bus: _____

I have the following boards and applications installed in my system: _____
_____
_____
I am encountering the following problem(s): _____
_____
_____
_____
and have received the following error messages/codes: _____
_____
_____
I have run the board diagnostics with the following results: _____
_____
You can reproduce the problem by performing these steps:
1. _____
_____
2. _____
_____
3. _____
_____

E-Mail and Fax Support

You can also get technical support by e-mailing or faxing the Technical Support Department:

- **E-mail**: You can reach Technical Support at the following address: tsupport@datx.com

  Ensure that you provide the following minimum information:

  – Your name,

  – Your company or organization,

  – A phone number,

  – An email address where you can be reached,

  – The hardware/software product you need help on,

  – A summary of the issue you are experiencing,

  – Your contract number, if applicable, and

  – Your product serial number or purchase date.

  Omitting any of the above information may delay our ability to resolve your issue.

- **Fax**: Please photocopy and complete the form on page 157, then fax Technical Support at the following number: (508) 481-8620.

Support requests from non-contract and out-of-warranty customers are processed with the same priority as telephone support requests.

World-Wide Web

For the latest tips, software fixes, and other product information, you can always access our World-Wide Web site free of charge at the following address: http://www.datatranslation.com

If Your Board Needs Factory Service

If your board must be returned to Data Translation, perform the following steps:

1. Record the board's serial number, then contact the Customer Service Department at (508) 481-3700 (if you are in the USA) and obtain a Return Material Authorization (RMA).
   If you are located outside the USA, call your local distributor for authorization and shipping instructions. The name and telephone number of your nearest distributor are listed in your Data Translation catalog.

   All return shipments to Data Translation must be marked with the correct RMA number to ensure proper processing.

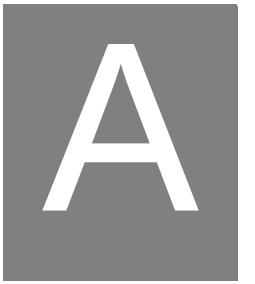
2. Using the original packing materials, if available, package the board as follows:

   – Wrap the board in an electrically conductive plastic material. Handle with ground protection. A static discharge can destroy components on the board.

   – Place in a secure shipping container.

3. Return the board to the following address, making sure the RMA number is visible on the outside of the box.

   Customer Service Dept.
   Data Translation, Inc.
   100 Locke Drive
   Marlboro, MA 01752-1192



Specifications

Table 8 lists the specifications for the A/D subsystem on the DT3010 Series boards.

Table 8: A/D Subsystem Specifications

Feature	DT3010, DT3010-268, DT3010/32, and DT3010/32-268 Specifications	DT3016 Specifications
Number of analog input channels Single-ended/ pseudo-differential: Differential:	 32 16	
Number of gains	4 (1, 2, 4, 8)	
Resolution	12 bits	16 bits
Data encoding Bipolar: Unipolar:	 Offset binary Binary	
System accuracy (full-scale) Gain = 1: Gain = 2: Gain = 4: Gain = 8:	 0.03% 0.04% 0.05% 0.05%	 0.01% 0.02% 0.02% 0.03%
Nonlinearity (integral)	±1.0 LSB	±2.0 LSB
Differential linearity	±0.75 LSB (no missing codes)	
Range Bipolar: Unipolar:	 ±10 V 0 to 10 V	

Table 8: A/D Subsystem Specifications (cont.)

Feature	DT3010, DT3010-268, DT3010/32, and DT3010/32-268 Specifications	DT3016 Specifications
Drift Zero: Gain:	 ±30 µV + (+15 µV * Gain)/°C ±30 ppm/°C	 ±20 µV + (+10 µV * Gain)/°C ±25 ppm/°C
Input impedance Off: On:	 100 MΩ, 10 pF 100 MΩ, 200 pF	 100 MΩ, 10 pF 100 MΩ, 200 pF
Input bias current	±20 nA	
Common mode voltage	±11 V maximum (operational)	
Maximum input voltage	±20 V maximum (protection)	
A/D converter noise	0.3 LSB rms	0.5 LSB rms
Amplifier input noise	15.0 µV rms + (20 µV rms * gain) 20.0 pA rms (current)	
Channel-to-channel offset	±40.0 µV	±30.0 µV
Channel acquisition time	1 µs to 0.05%	4 µs to 0.01%
A/D conversion time	0.8 µs	4.0 µs
Effective number of bits @ 1 kHz sine wave, 2 channels: 10 kHz sine wave, 2 channels: sine wave, 2 channels:	 11.7 bits typical (1 MS/s aggregate rate) 11.6 bits typical (1 MS/s aggregate rate) 11.5 bits typical (1 MS/s aggregate rate with sine wave of 40 kHz)	 14.4 bits typical (at 150 kS/s aggregate rate) 14.2 bits typical (at 150 kS/s aggregate rate) 13.5 bits typical (at 150 kS/s aggregate rate with sine wave of 20 kHz)

Table 8: A/D Subsystem Specifications (cont.)

Feature	DT3010, DT3010-268, DT3010/32, and DT3010/32-268 Specifications	DT3016 Specifications
Total Harmonic Distortion @ 1 kHz input	–71 dB typical (at 1.25 MS/s rate)	–82 dB typical (at 250 kS/s rate)
Channel crosstalk	–80 dB @ 1 kHz	
Data throughput		
Single channel:	1.25 MSamples/s, 0.03% accuracy;	250 kSamples/s, 0.01% accuracy;
Multiple channel (scan):	1.0 MSamples/s, 0.05% accuracy; 750 kSamples/s, 0.03% accuracy	200 kSamples/s, 0.03% accuracy; 150 kSamples/s, 0.01% accuracy
External A/D sample clock		
Input type:	Schmitt trigger, falling-edge sensitive	Schmitt trigger, falling-edge sensitive
Input load:	1 HCT14 (TTL)	1 HCT14 (TTL)
High-level input voltage:	2.0 V minimum	2.0 V minimum
Low-level input voltage:	0.8 V maximum	0.8 V maximum
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)	0.4 V (minimum); 1.5 V (maximum)
High-level input current:	1.0 µA	1.0 µA
Low-level input current:	–1.0 µA	–1.0 µA
Minimum pulse width:	100 ns (high); 150 ns (low)	100 ns (high); 150 ns (low)
Maximum frequency:	1.25 MHz	250 kHz
Termination:	22 kΩ resistor pullup to 5 V	22 kΩ resistor pullup to 5 V

Table 8: A/D Subsystem Specifications (cont.)

Feature	DT3010, DT3010-268, DT3010/32, and DT3010/32-268 Specifications	DT3016 Specifications
External A/D digital (TTL) trigger		
Input type:	Schmitt trigger, falling-edge sensitive	
Input load:	1 HCT14 (TTL)	
High-level input voltage:	2.0 V minimum	
Low-level input voltage:	0.8 V maximum	
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)	
High-level input current:	1.0 µA	
Low-level input current:	–1.0 µA	
Minimum pulse width:	100 ns (high); 100 ns (low)	
Termination:	22 kΩ resistor pullup to +5 V	
External analog trigger		
Input type:	Threshold sensitive	
Threshold voltage:	Programmable	
Threshold range:	–10 V to +10 V (includes TTL)	
Threshold resolution:	8 bits/78 mV per LSB	
Hysteresis:	50 mV typical	
Input impedance:	12 kΩ/20 pF typical	
Maximum input voltage:	±20 V	
Minimum pulse width:	100 ns (high); 100 ns (low)	

Table 8: A/D Subsystem Specifications (cont.)

Feature	DT3010, DT3010-268, DT3010/32, and DT3010/32-268 Specifications	DT3016 Specifications
A/D sample clock output signal		
Output driver:	ALS244 (TTL)	
Output driver high voltage:	2.0 V minimum (IOH = –15 mA); 2.4 V minimum (IOH = –3 mA)	
Output driver low voltage:	0.5 V maximum (IOL = 24 mA); 0.4 V maximum (IOL = 12 mA)	
Termination:	22 Ω series resistor	
A/D trigger output signal		
Output driver:	ALS244 (TTL)	
Output driver high voltage:	2.0 V minimum (IOH = –15 mA); 2.4 V minimum (IOH = –3 mA)	
Output driver low voltage:	0.5 V maximum (IOL = 24 mA); 0.4 V maximum (IOL = 12 mA)	
Termination:	22 Ω series resistor	

Table 8: A/D Subsystem Specifications (cont.)

Feature	DT3010, DT3010-268, DT3010/32, and DT3010/32-268 Specifications	DT3016 Specifications
Dynamic Digital Output Channels		
Number of channels:	2	
Output driver:	ALS244 (TTL)	
Output driver high voltage:	2.0 V minimum (IOH = –15 mA); 2.4 V minimum (IOH = –3 mA)	
Output driver low voltage:	0.5 V maximum (IOL = 24 mA); 0.4 V maximum (IOL = 12 mA)	
Termination:	22 Ω series resistor	

Table 9 lists the specifications for the D/A subsystem on the DT3010 Series boards.

Table 9: D/A Subsystem Specifications

Feature	DT3010, DT3010/32, and DT3010/32-268 Specifications	DT3016 Specifications
Number of analog output channels	2 (voltage output)	
Resolution	12 bits	16 bits
Data encoding (input)	Offset binary	
Nonlinearity (integral)	±1.0 LSB	±4.0 LSB
Differential linearity	±0.75 LSB (monotonic)	
Output range	±10 V (bipolar)	

Table 9: D/A Subsystem Specifications (cont.)

Feature	DT3010, DT3010/32, and DT3010/32-268 Specifications	DT3016 Specifications
Error Zero: Gain:	Adjustable to 0 Adjustable to 0	
Throughput Full scale: 100 mV Step, continuously paced: 100 mV Step, waveform mode:	 200 kSamples/s maximum per channel 500 kSamples/s maximum per channel (system-dependent) 500 kSamples/s maximum per channel	 100 kSamples/s maximum per channel 200 kSamples/s maximum per channel (system-dependent) 200 kSamples/s maximum per channel
Current output	±5 mA maximum load	
Output impedance	0.1 Ω maximum	
Capacitive drive capability	0.004 µF (no oscillators)	
Protection	Short circuit to Analog Common	
Power-on voltage	0 V ±10 mV maximum	
Settling time to 0.01% of FSR	5 µs, 20 V step; 2.0 µs, 100 mV step	10 µs, 20 V step; 5.0 µs, 100 mV step
Slew rate	10 V/ µs	5 V/ µs

Table 9: D/A Subsystem Specifications (cont.)

Feature	DT3010, DT3010/32, and DT3010/32-268 Specifications	DT3016 Specifications
Filters	–	20 kHz (software-selectable)
External D/A sample clock		
Input type:	Schmitt trigger, falling-edge sensitive	Schmitt trigger, falling-edge sensitive
Input load:	1 HCT14 (TTL)	1 HCT14 (TTL)
High-level input voltage:	2.0 V minimum	2.0 V minimum
Low-level input voltage:	0.8 V maximum	0.8 V maximum
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)	0.4 V (minimum); 1.5 V (maximum)
High-level input current:	1.0 µA	1.0 µA
Low-level input current:	–1.0 µA	–1.0 µA
Minimum pulse width:	200 ns (high); 150 ns (low)	200 ns (high); 150 ns (low)
Maximum frequency:	500 kHz	200 kHz
Termination:	22 kΩ resistor pullup to 5 V	22 kΩ resistor pullup to 5 V
External D/A digital (TTL) trigger		
Input type:	Schmitt trigger, edge sensitive	
Input load:	1 HCT14 (TTL)	
High-level input voltage:	2.0 V minimum	
Low-level input voltage:	0.8 V maximum	
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)	
High-level input current:	1.0 µA	
Low-level input current:	–1.0 µA	
Minimum pulse width:	100 ns (high); 100 ns (low)	
Termination:	22 kΩ resistor pullup to +5 V	

Table 10 lists the specifications for the DIN / DOUT subsystems on the DT3010 Series boards.

Table 10: DIN/DOUT Subsystem Specifications

Feature	Specifications
Number of lines	16 (bidirectional)
Number of ports	2 (8 bits each)
Termination	22 kΩ resistor pullup to +5 V; 22 Ω series resistor
Inputs Input type: Input load: High-level input voltage: Low-level input voltage: High-level input current: Low-level input current:	 Level sensitive 1 ALS652 (TTL), 1 ALS374 (TTL) 2.0 V minimum 0.8 V maximum 20 µA –0.2 mA
Outputs Output driver: Output driver high voltage: Output driver low voltage:	 ALS652 (TTL) 2.0 V minimum (IOH = –15 mA); 2.4 V minimum (IOH = –3 mA) 0.5 V maximum (IOL = 24 mA); 0.4 V maximum (IOL = 12 mA)

Table 11 lists the specifications for the C/T subsystems on the DT3010 Series boards.

Table 11: C/T Subsystem Specifications

Feature	Specifications
Number of counter/timers	4
Clock Inputs	
Input type:	Schmitt trigger, rising-edge sensitive
Input load:	1 HCT14 (TTL)
High-level input voltage:	2.0 V minimum
Low-level input voltage:	0.8 V maximum
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)
High-level input current:	1.0 µA
Low-level input current:	–1.0 µA
Minimum pulse width:	100 ns (high); 100 ns (low)
Maximum frequency:	5.0 MHz
Termination:	22 kΩ resistor pullup to +5 V
Gate Inputs	
Input type:	Schmitt trigger, level sensitive
Input load:	1 HCT14 (TTL)
High-level input voltage:	2.0 V minimum
Low-level input voltage:	0.8 V maximum
Hysteresis:	0.4 V (minimum); 1.5 V (maximum)
High-level input current:	1.0 µA
Low-level input current:	–1.0 µA
Minimum pulse width:	100 ns (high); 100 ns (low)
Maximum frequency:	5.0 MHz
Termination:	22 kΩ resistor pullup to +5 V

Table 11: C/T Subsystem Specifications (cont.)

Feature	Specifications
Counter Outputs	
Output driver:	ALS244 (TTL)
Output driver high voltage:	2.0 V minimum (IOH = –15 mA); 2.4 V minimum (IOH = –3 mA)
Output driver low voltage:	0.5 V maximum (IOL = 24 mA); 0.4 V maximum (IOL = 12 mA)
Termination:	22 Ω series resistor

Table 12 lists the power, physical, and environmental specifications for the DT3010 Series boards.

Table 12: Power, Physical, and Environmental Specifications

Feature	Specifications
Power	
+5 V (±0.25 V)	1.5 A nominal
– 5 V	not used
+12 V	0.12 A nominal
–12 V	0.1 A nominal
Physical	
Dimensions:	8.5 inches (length) by 4.2 inches (width)
Weight:	5.95 ounces (170 grams)
Environmental	
Operating temperature range:	0°C to 70°C
Storage temperature range:	–25°C to 85°C
Relative humidity:	To 95%, noncondensing

Table 13 lists the connector specifications for the DT3010, DT3010/32, DT3010/32-268, and DT3016 boards and corresponding cables.

Table 13: Connector Specifications for the DT3010, DT3010/32, DT3010/32,-268, and DT3016

Feature	Specifications
50-Pin Connector	
Plug for cable:	AMP#787131-1
Cable shell kit:	AMP#787133-2
Termination covers:	AMP#787056-1 (included with kit)
Cable wire:	AMP#57506-1
Receptacle for board:	AMP#787096-1
Latching posts:	AMP#787003-3 (bag of 200)
68-Pin Connector	
Plug for cable:	AMP#787131-3
Cable shell kit:	AMP#787229-2
Termination covers:	AMP#787131-3 (included with kit)
Cable wire:	AMP#57508-1
Receptacle for board:	AMP#787254-1
Latching posts:	AMP#787003-3 (bag of 200)

Table 14 lists the connector specifications for the DT3010-268 board and corresponding cables.

Table 14: Connector Specifications for the DT3010-268 Board

Feature	Specifications
68-Pin Connector	
Receptacle for EP324:	AMP#1-111196-7
	AMP#749877-7
2 Screwlocks for EP324:	AMP#750644-1
6 foot DB68 male to DB68 male (EP325):	AMP#621885-2
Receptacle for board:	AMP#787362-7
2 Screwlocks for board:	AMP#750644-1
Header for board:	AMP#1-104068-8

B

Connector Pin Assignments

Table 15 lists the pin assignments of connector J1 on the DT3010, DT3010/32, DT3010/32-268, and DT3016 boards.

Table 15: Connector J1 Pin Assignments on the DT3010, DT3010/32, DT3010/32-268, and DT3016 Boards

Pin Number	Signal Description	Pin Number	Signal Description
1	+5 V Ref_Out	2	Reserved
3	Reserved	4	Analog Output 1+
5	Analog Output 0+	6	–15 V output
7	+15 V output	8	Shield Ground
9	Amp Low	10	Analog Input 23/ Analog Input 15 Return
11	Analog Input 22/ Analog Input 14 Return	12	Analog Input 21/ Analog Input 13 Return
13	Analog Input 20/ Analog Input 12 Return	14	Analog Input 19/ Analog Input 11 Return
15	Analog Input 18/ Analog Input 10 Return	16	Analog Input 17/ Analog Input 09 Return
17	Analog Input 16/ Analog Input 8 Return	18	Analog Input 7
19	Analog Input 6	20	Analog Input 5
21	Analog Input 4	22	Analog Input 3
23	Analog Input 2	24	Analog Input 1
25	Analog Input 0	26	Analog Ground
27	Reserved	28	Reserved
29	Analog Output 1 Return	30	Analog Output 0 Return
31	Reserved	32	Power Ground

Table 15: Connector J1 Pin Assignments on the DT3010, DT3010/32, DT3010/32-268, and DT3016 Boards (cont.)

Pin Number	Signal Description	Pin Number	Signal Description
33	Shield Ground	34	Analog Ground
35	Analog Input 31/ Analog Input 15 Return	36	Analog Input 30/ Analog Input 14 Return
37	Analog Input 29/ Analog Input 13 Return	38	Analog Input 28/ Analog Input 12 Return
39	Analog Input 27/ Analog Input 11 Return	40	Analog Input 26/ Analog Input 10 Return
41	Analog Input 25/ Analog Input 09 Return	42	Analog Input 24/ Analog Input 08 Return
43	Analog Input 15/ Analog Input 7 Return	44	Analog Input 14/ Analog Input 6 Return
45	Analog Input 13/ Analog Input 5 Return	46	Analog Input 12/ Analog Input 4 Return
47	Analog Input 11/ Analog Input 3 Return	48	Analog Input 10/ Analog Input 2 Return
49	Analog Input 9/ Analog Input 1 Return	50	Analog Input 8/ Analog Input 0 Return

Table 16 lists the pin assignments of connector J2 on the DT3010, DT3010/32, DT3010/32-268, and DT3016 boards.

Table 16: Connector J2 Pin Assignments on the DT3010, DT3010/32, DT3010/32-268, and DT3016 Boards

Pin Number	Signal Description	Pin Number	Signal Description
1	+ 5 V Output	2	+ 5 V Output
3	Reserved	4	A/D Sample Clock Output
5	A/D Trigger Output	6	External A/D TTL Trigger
7	External A/D Sample Clock Input	8	External D/A TTL Trigger
9	External D/A Clock Input	10	User Counter Output 3
11	User Clock Input 3	12	User Counter Output 2
13	User Clock Input 2	14	User Counter Output 1
15	User Clock Input 1	16	User Counter Output 0
17	User Clock Input 0	18	Digital Ground
19	Digital I/O Bank B 3	20	Digital I/O Bank B 2
21	Digital I/O Bank B 1	22	Digital I/O Bank B 0
23	Digital Ground	24	Digital I/O Bank A 3
25	Digital I/O Bank A 2	26	Digital I/O Bank A 1
27	Digital I/O Bank A 0	28	Digital Ground
29	Dynamic Digital Output 1	30	Dynamic Digital Output 0
31	Reserved	32	Reserved
33	Shield Ground	34	Analog Trigger
35	Digital Ground	36	Digital Ground
37	Reserved	38	Digital Ground
39	Digital Ground	40	Digital Ground
41	Digital Ground	42	Digital Ground

Table 16: Connector J2 Pin Assignments on the DT3010, DT3010/32, DT3010/32-268, and DT3016 Boards (cont.)

Pin Number	Signal Description	Pin Number	Signal Description
43	Digital Ground	44	External Gate 3
45	Digital Ground	46	External Gate 2
47	Digital Ground	48	External Gate 1
49	Digital Ground	50	External Gate 0
51	Digital Ground	52	Digital Ground
53	Digital I/O Bank B 7	54	Digital I/O Bank B 6
55	Digital I/O Bank B 5	56	Digital I/O Bank B 4
57	Digital Ground	58	Digital I/O Bank A 7
59	Digital I/O Bank A 6	60	Digital I/O Bank A 5
61	Digital I/O Bank A 4	62	Digital Ground
63	Digital Ground	64	Digital Ground
65	Reserved	66	Reserved
67	Shield Ground	68	Analog Trigger Return

Table 17 lists the pin assignments of connector J1 on the DT3010-268 board.

Table 17: Connector J1 Pin Assignments on the DT3010-268 Board

Pin Number	Signal Description	Pin Number	Signal Description
1	+5 V Output	2	User Counter Output 1
3	User Counter Output 0	4	Digital Ground
5	User Clock Input 0	6	Digital I/O Bank A3
7	Digital I/O Bank A2	8	Digital I/O Bank A1
9	Digital I/O Bank A0	10	External D/A TTL Trigger
11	+15 V Output	12	–15 V Output
13	External A/D Sample Input	14	External A/D TTL Trigger
15	Analog Trigger	16	Analog Output 1+
17	Analog Output 0+	18	Amp Low
19	Analog Input 23/ Analog Input 15 Return	20	Analog Input 22/ Analog Input 14 Return
21	Analog Input 21/ Analog Input 13 Return	22	Analog Input 20/ Analog Input 12 Return
23	Analog Input 19/ Analog Input 11 Return	24	Analog Input 18/ Analog Input 10 Return
25	Analog Input 17/ Analog Input 09 Return	26	Analog Input 16/ Analog Input 08 Return
27	Analog Input 07	28	Analog Input 06
29	Analog Input 05	30	Analog Input 04
31	Analog Input 03	32	Analog Input 02
33	Analog Input 01	34	Analog Input 00
35	Digital Ground	36	External Gate 1
37	External Gate 0	38	User Clock Input 1

Table 17: Connector J1 Pin Assignments on the DT3010-268 Board (cont.)

Pin Number	Signal Description	Pin Number	Signal Description
39	Digital Ground	40	Digital I/O Bank A7
41	Digital I/O Bank A6	42	Digital I/O Bank A5
43	Digital I/O Bank A4	44	External D/A Clock Input
45	Power Ground	46	A/D Trigger Output
47	A/D Sample Clock Output	48	External A/D Trigger and Clock Enable
49	Analog Ground	50	+5 V Ref_Out
51	Analog Output 0 Ground	52	Analog Ground
53	Analog Input 31/ Analog Input 23 Return	54	Analog Input 30/ Analog Input 22 Return
55	Analog Input 29/ Analog Input 21 Return	56	Analog Input 28/ Analog Input 20 Return
57	Analog Input 27/ Analog Input 19 Return	58	Analog Input 26/ Analog Input 18 Return
59	Analog Input 25/ Analog Input 17 Return	60	Analog Input 24/ Analog Input 16 Return
61	Analog Input 15/ Analog Input 07 Return	62	Analog Input 14/ Analog Input 06 Return
63	Analog Input 13/ Analog Input 05 Return	64	Analog Input 12/ Analog Input 04 Return
65	Analog Input 11/ Analog Input 03 Return	66	Analog Input 10/ Analog Input 02 Return
67	Analog Input 09/ Analog Input 01 Return	68	Analog Input 08/ Analog Input 00 Return

Table 18 lists the pin assignments of connector J2 on the DT3010-268 board.

Table 18: Connector J2 Pin Assignments on the DT3010-268 Board

Pin Number	Signal Description	Pin Number	Signal Description
1	+5 V Output	2	User Counter Output 3
3	User Counter Output 2	4	Digital Ground
5	User Clock Input 2	6	Digital I/O Bank B3
7	Digital I/O Bank B2	8	Digital I/O Bank B1
9	Digital I/O Bank B0	10	Reserved
11	Reserved	12	Reserved
13	Dynamic Digital Output 0	14	Dynamic Digital Output 1
15	Reserved	16	Reserved
17	Reserved	18	Reserved
19	Reserved	20	Reserved
21	Reserved	22	Reserved
23	Reserved	24	Reserved
25	Reserved	26	Reserved
27	Reserved	28	Reserved
29	Reserved	30	Reserved
31	Reserved	32	Reserved
33	Reserved	34	Reserved
35	Digital Ground	36	External Gate 3
37	External Gate 2	38	User Clock Input 3

Table 18: Connector J2 Pin Assignments on the DT3010-268 Board (cont.)

Pin Number	Signal Description	Pin Number	Signal Description
39	Digital Ground	40	Digital I/O Bank B7
41	Digital I/O Bank B6	42	Digital I/O Bank B5
43	Digital I/O Bank B4	44	Reserved
45	Reserved	46	Reserved
47	Reserved	48	Digital Ground
49	Reserved	50	Reserved
51	Reserved	52	Reserved
53	Reserved	54	Reserved
55	Reserved	56	Reserved
57	Reserved	58	Reserved
59	Reserved	60	Reserved
61	Reserved	62	Reserved
63	Reserved	64	Reserved
65	Reserved	66	Reserved
67	Reserved	68	Reserved

Table 19 lists the screw terminal assignments for connector J1 on the DT740 screw terminal panel.

Table 19: Pin Assignments for Connector J1 on the DT740

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
1	25	Analog Input 00	2	50	Analog Input 08/00 Return
3	24	Analog Input 01	4	49	Analog Input 09/01 Return
5	23	Analog Input 02	6	48	Analog Input 10/02 Return
7	22	Analog Input 03	8	47	Analog Input 11/03 Return
9	21	Analog Input 04	10	46	Analog Input 12/04 Return
11	20	Analog Input 05	12	45	Analog Input 13/05 Return
13	19	Analog Input 06	14	44	Analog Input 14/06 Return
15	18	Analog Input 07	16	43	Analog Input 15/07 Return
17	17	Analog Input 16/08	18	42	Analog Input 24/08 Return
19	16	Analog Input 17/09	20	41	Analog Input 25/09 Return
21	15	Analog Input 18/10	22	40	Analog Input 26/10 Return
23	14	Analog Input 19/11	24	39	Analog Input 27/11 Return
25	13	Analog Input 20/12	26	38	Analog Input 28/12 Return
27	12	Analog Input 21/13	28	37	Analog Input 29/13 Return
29	11	Analog Input 22/14	30	36	Analog Input 30/14 Return
31	10	Analog Input 23/15	32	35	Analog Input 31/15 Return
33	9	Amp Low	34	34	Analog Ground
35	8	Analog Shield Ground	36	33	Analog Shield Ground
37	7	+15 V Output	38	32	Power Ground
39	6	–15 V Output	40	31	Reserved
41	5	Analog Output 0+	42	30	Analog Output 0 Return
43	4	Analog Output 1+	44	29	Analog Output 1 Return

Table 19: Pin Assignments for Connector J1 on the DT740 (cont.)

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
45	3	Reserved	46	28	Reserved
47	2	Reserved	48	27	Reserved
49	1	+5 V Reference Out	50	26	Analog Ground
51	-	Analog Shield Ground	52	-	Analog Shield Ground
53	-	Analog Shield Ground	54	-	Analog Shield Ground
55	-	Analog Shield Ground	56	-	Analog Shield Ground

Table 20 lists the screw terminal assignments for connector J2 on the DT740 screw terminal panel.

Table 20: Screw Terminal Assignments for Connector J2 on the DT740 Screw Terminal Panel

TB #	J2 Pin #	Signal Description	TB #	J2 Pin #	Signal Description
57	51, 52	Digital Ground	58	17	User Clock Input 0
59	16	User Counter Output 0	60	50	External Gate 0
61	49	Digital Ground	62	15	User Clock Input 1
63	14	User Counter Output 1	64	48	External Gate 1
65	47	Digital Ground	66	13	User Clock Input 2
67	12	User Counter Output 2	68	46	External Gate 2
69	45	Digital Ground	70	11	User Clock Input 3
71	10	User Counter Output 3	72	44	External Gate 3
73	43	Digital Ground	74	9	External D/A Sample Clock In

Table 20: Screw Terminal Assignments for Connector J2 on the DT740 Screw Terminal Panel (cont.)

TB #	J2 Pin #	Signal Description	TB #	J2 Pin #	Signal Description
75	8	External D/A TTL Trigger	76	7	External A/D Sample Clock In
77	6	External A/D TTL Trigger	78	5	A/D Trigger Out
79	4	A/D Sample Clock Out	80	3	Reserved
81	23, 28, 42	Digital Ground	82	39, 41, 57, 62	Digital Ground
83	18, 38, 40, 63, 64	Digital Ground	84	65	Reserved
85	31	Reserved	86	37	Reserved
87	30	Dynamic Digital Output 0	88	29	Dynamic Digital Output 1
89	27	Digital I/O Bank A 0	90	26	Digital I/O Bank A 1
91	25	Digital I/O Bank A 2	92	24	Digital I/O Bank A 3
93	61	Digital I/O Bank A 4	94	60	Digital I/O Bank A 5
95	59	Digital I/O Bank A 6	96	58	Digital I/O Bank A 7
97	22	Digital I/O Bank B 0	98	21	Digital I/O Bank B 1
99	20	Digital I/O Bank B 2	100	19	Digital I/O Bank B 3
101	56	Digital I/O Bank B 4	102	55	Digital I/O Bank B 5
103	54	Digital I/O Bank B 6	104	53	Digital I/O Bank B 7
105	33	Digital Shield Ground	106	68	Analog Ground

Table 20: Screw Terminal Assignments for Connector J2 on the DT740 Screw Terminal Panel (cont.)

TB #	J2 Pin #	Signal Description	TB #	J2 Pin #	Signal Description
107	34	Analog Trigger	108	67	Digital Shield Ground
109	32	Reserved	110	66	Reserved
111	35, 36	Digital Ground	112	1, 2	+5 V Out

Table 21 lists the screw terminal assignments for connector J1 on the STP268 screw terminal panel.

Table 21: Screw Terminal Assignments for Connector J1 on the STP268

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
1	34	Analog Input 00	2	68	Analog Input 08/ Analog Input 00 Return
3	33	Analog Input 01	4	67	Analog Input 09/ Analog Input 01 Return
5	32	Analog Input 02	6	66	Analog Input 10/ Analog Input 02 Return
7	31	Analog Input 03	8	65	Analog Input 11/ Analog Input 03 Return
9	30	Analog Input 04	10	64	Analog Input 12/ Analog Input 04 Return
11	29	Analog Input 05	12	63	Analog Input 13/ Analog Input 05 Return
13	28	Analog Input 06	14	62	Analog Input 14/ Analog Input 06 Return

Table 21: Screw Terminal Assignments for Connector J1 on the STP268

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
15	27	Analog Input 07	16	61	Analog Input 15/ Analog Input 07 Return
17	26	Analog Input 16	18	60	Analog Input 24/ Analog Input 16 Return
19	25	Analog Input 17	20	59	Analog Input 25/ Analog Input 17 Return
21	24	Analog Input 18	22	58	Analog Input 26/ Analog Input 18 Return
23	23	Analog Input 19	24	57	Analog Input 27/ Analog Input 19 Return
25	22	Analog Input 20	26	56	Analog Input 28/ Analog Input 20 Return
27	21	Analog Input 21	28	55	Analog Input 29/ Analog Input 21 Return
29	20	Analog Input 22	30	54	Analog Input 30/ Analog Input 22 Return
31	19	Analog Input 23	32	53	Analog Input 31/ Analog Input 23 Return
33	18	Amp Low	34	49	Analog Ground
35	11	+15 V Output	36	45	Power Ground
37	12	–15 V Output	38	46	A/D Trigger Output
39	15	Analog Trigger	40	52	Analog Ground
41	17	Analog Output 0+	42	51	Analog Output Ground
43	16	Analog Output 1+	44	50	+5 Volts_Ref Output
45	10	External D/A TTL Trigger	46	44	External D/A Clock Input

Table 21: Screw Terminal Assignments for Connector J1 on the STP268

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
47	47	A/D Sample Clock Output	48	13	External A/D Sample Clock Input
49	14	External A/D TTL Trigger	50	48	External A/D Trigger and Clock Enable
51	35	Digital Ground	52	1	+5 V Output
53	39	Digital Ground	54	5	User Clock Input 0
55	3	User Counter Output 0	56	37	External Gate 0
57	4	Digital Ground	58	38	User Clock Input 1
59	2	User Counter Output 1	60	36	External Gate 1
61	9	Digital I/O Bank A0	62	8	Digital I/O Bank A1
63	7	Digital I/O Bank A2	64	6	Digital I/O Bank A3
65	43	Digital I/O Bank A4	66	42	Digital I/O Bank A5
67	41	Digital I/O Bank A6	68	40	Digital I/O Bank A7

Table 22 lists the screw terminal assignments for connector J2 on the STP268 screw terminal panel.

Table 22: Screw Terminal Assignments for Connector J2 on the STP268

TB #	J2 Pin #	SIgnal Description	TB #	J2 Pin #	Signal Description
1	–	Reserved	2	–	Reserved
3	–	Reserved	4	–	Reserved
5	–	Reserved	6	–	Reserved

Table 22: Screw Terminal Assignments for Connector J2 on the STP268

TB #	J2 Pin #	SIgnal Description	TB #	J2 Pin #	Signal Description
7	–	Reserved	8	–	Reserved
9	–	Reserved	10	–	Reserved
11	–	Reserved	12	–	Reserved
13	–	Reserved	14	–	Reserved
15	–	Reserved	16	–	Reserved
17	–	Reserved	18	–	Reserved
19	–	Reserved	20	–	Reserved
21	–	Reserved	22	–	Reserved
23	–	Reserved	24	–	Reserved
25	–	Reserved	26	–	Reserved
27	–	Reserved	28	–	Reserved
29	–	Reserved	30	–	Reserved
31	–	Reserved	32	–	Reserved
33	–	Reserved	34	–	Reserved
35	–	Reserved	36	–	Reserved
37	–	Reserved	38	–	Reserved
39	–	Reserved	40	–	Reserved
41	–	Reserved	42	–	Reserved
43	–	Reserved	44	–	Reserved
45	–	Reserved	46	–	Reserved
47	–	Reserved	48	13	Dynamic Digital Output 0

Table 22: Screw Terminal Assignments for Connector J2 on the STP268

TB #	J2 Pin #	SIgnal Description	TB #	J2 Pin #	Signal Description
49	14	Dynamic Digital Output 1	50	4, 35, 39	Digital Ground
51	4, 35, 39	Digital Ground	52	1	+5 V Output
53	4, 35, 39	Digital Ground	54	5	User Clock Input 2
55	3	User Counter Output 2	56	37	External Gate 2
57	4, 35, 39	Digital Ground	58	38	User Clock Input 3
59	2	User Counter Output 3	60	36	External Gate 3
61	9	Digital I/O Bank B0	62	8	Digital I/O Bank B1
63	7	Digital I/O Bank B2	64	6	Digital I/O Bank B3
65	43	Digital I/O Bank B4	66	42	Digital I/O Bank B5
67	41	Digital I/O Bank B6	68	40	Digital I/O Bank B7

Table 23 lists the screw terminal assignments for connector J1 on the STP268-EC screw terminal panel.

Table 23: Screw Terminal Assignments for Connector J1 on the STP268-EC

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
1	1	+5 V Output	2	2	User Counter Output 1
3	3	User Counter Output 0	4	4	Digital Ground
5	5	User Clock Input 0	6	6	Digital I/O Bank A3

Table 23: Screw Terminal Assignments for Connector J1 on the STP268-EC

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
7	7	Digital I/O Bank A2	8	8	Digital I/O Bank A1
9	9	Digital I/O Bank A0	10	10	External D/A TTL Trigger
11	11	+15 V Output	12	12	–15 V Output
13	13	External A/D Sample Input	14	14	External A/D TTL Trigger
15	15	Analog Trigger	16	16	Analog Output 1+
17	17	Analog Output 0+	18	18	Amp Low
19	19	Analog Input 23	20	20	Analog Input 22
21	21	Analog Input 21	22	22	Analog Input 20/
23	23	Analog Input 19	24	24	Analog Input 18
25	25	Analog Input 17	26	26	Analog Input 16
27	27	Analog Input 07	28	28	Analog Input 06
29	29	Analog Input 05	30	30	Analog Input 04
31	31	Analog Input 03	32	32	Analog Input 02
33	33	Analog Input 01	34	34	Analog Input 00
35	35	Digital Ground	36	36	External Gate 1
37	37	External Gate 0	38	38	User Clock Input 1
39	39	Digital Ground	40	40	Digital I/O Bank A7
41	41	Digital I/O Bank A6	42	42	Digital I/O Bank A5
43	43	Digital I/O Bank A4	44	44	External D/A Clock Input
45	45	Power Ground	46	46	A/D Trigger Output
47	47	A/D Sample Clock Output	48	48	External A/D Trigger and Clock Enable

Table 23: Screw Terminal Assignments for Connector J1 on the STP268-EC

TB #	J1 Pin #	Signal Description	TB #	J1 Pin #	Signal Description
49	49	Analog Ground	50	50	+5 V Ref_Out
51	51	Analog Output Ground	52	52	Analog Ground
53	53	Analog Input 31/ Analog Input 23 Return	54	54	Analog Input 30/ Analog Input 22 Return
55	55	Analog Input 29/ Analog Input 21 Return	56	56	Analog Input 28/ Analog Input 20 Return
57	57	Analog Input 27/ Analog Input 19 Return	58	58	Analog Input 26/ Analog Input 18 Return
59	59	Analog Input 25/ Analog Input 17 Return	60	60	Analog Input 24/ Analog Input 16 Return
61	61	Analog Input 15/ Analog Input 07 Return	62	62	Analog Input 14/ Analog Input 06 Return
63	63	Analog Input 13/ Analog Input 05 Return	64	64	Analog Input 12/ Analog Input 04 Return
65	65	Analog Input 11/ Analog Input 03 Return	66	66	Analog Input 10/ Analog Input 02 Return
67	67	Analog Input 09/ Analog Input 01 Return	68	68	Analog Input 08/ Analog Input 00 Return

Table 24 lists the screw terminal assignments for connector J2 on the STP268-EC screw terminal panel.

Table 24: Screw Terminal Assignments for Connector J2 on the STP268-EC

TB #	J2 Pin #	Signal Description	TB #	J2 Pin #	Signal Description
6	41	Digital I/O 3	7	43	Digital I/O 2
8	45	Digital I/O 1	9	47	Digital I/O 0
40	33	Digital I/O 7	41	35	Digital I/O 6
42	37	Digital I/O 5	43	39	Digital I/O 4

Table 25 lists the screw terminal assignments for connector J3 on the STP268-EC screw terminal panel.

Table 25: Screw Terminal Assignments for Connector J3 on the STP268-EC

TB #	J3 Pin #	SIgnal Description	TB #	J3 Pin #	Signal Description
16	22	DAC1_OUT[a]	17	20	DAC0_OUT[b]
18	25	Amp Low	–	26	Not Connected
27	23	Analog Input 07	28	19	Analog Input 06
29	17	Analog Input 05	30	13	Analog Input 04
31	11	Analog Input 03	32	7	Analog Input 02
33	5	Analog Input 01	34	1	Analog Input 00
51	21, 24	Analog Ground[c]	52	3, 6, 9, 12, 15, 18, 21, 24	Analog Ground
61	22	Analog Input 15[d] Analog Input 07 Return	62	20	Analog Input 14[e]/ Analog Input 06 Return

Table 25: Screw Terminal Assignments for Connector J3 on the STP268-EC

TB #	J3 Pin #	SIgnal Description	TB #	J3 Pin #	Signal Description
63	16	Analog Input 13/ Analog Input 05 Return	64	14	Analog Input 12/ Analog Input 04 Return
65	10	Analog Input 11/ Analog Input 03 Return	66	8	Analog Input 10/ Analog Input 02 Return
67	4	Analog Input 09/ Analog Input 01 Return	68	2	Analog Input 08/ Analog Input 00 Return

a. Jumper W3 must be installed on the STP268-EC. If this jumper is not installed, this signal is not available through this connector.

b. Jumper W2 must be installed on the STP268-EC. If this jumper is not installed, this signal is not available through this connector.

c. Jumper W1 must be installed on the STP268-EC for DAC0 Ground; jumper W4 must be installed on the STP268-EC for DAC1 Ground. If these jumpers are not installed, this signal is not available through this connector.

d. If jumper W3 is installed on the STP268-EC, this signal is not available through this connector.

e. If jumper W2 is installed on the STP268-EC, this signal is not available through this connector.

Table 26 lists the screw terminal assignments for connector J4 on the STP268-EC screw terminal panel.

Table 26: Screw Terminal Assignments for Connector J4 on the STP268-EC

TB #	J4 Pin #	SIgnal Description	TB #	J4 Pin #	SIgnal Description
19	23	Analog Input 23	20	19	Analog Input 22
21	17	Analog Input 21	22	13	Analog Input 20
23	11	Analog Input 19	24	7	Analog Input 18
25	5	Analog Input 17	26	1	Analog Input 16
52	3, 6, 9, 12, 15, 18, 21, 24	Analog Ground	53	22	Analog Input 31 Analog Input 23 Return
54	20	Analog Input 30 Analog Input 22 Return	55	16	Analog Input 29 Analog Input 21 Return
56	14	Analog Input 28 Analog Input 20 Return	57	10	Analog Input 27 Analog Input 19 Return
58	8	Analog Input 26 Analog Input 18 Return	59	4	Analog Input 25 Analog Input 17 Return
60	2	Analog Input 24 Analog Input 16 Return	–	25	Not Connected
–	26	Not Connected			

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